National Exams December 2008

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination, however, candidates are allowed to bring the following into the examination room.
   (i) One hand-written information sheet (8.5" X 11") of self prepared notes.

3. This paper contains **SIX (6)** questions and comprises **eight (8)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and marks for each question part are indicated in brackets.

7. Data on some relevant Digital ICs are provided in the Appendix.

8. A PAL16L8 Data sheet is provided on page 8 (in the Appendix). It can be used to provide the solution of Problem 2, part (a) and should be attached to your answer sheet.

1. Provide a brief answer for the following questions with justification.

a) Which of the following binary values is closest to the decimal value $(1.02)_{10}$. Justify your answer

i. $(1.01)_2$ ii. $(1.0001)_2$
iii. $(1.00000101)_2$ iv. $(1.0101001)_2$

(6 marks)

b) If a digital system has 6 inputs, how many possible input combinations are there?

(2 marks)

c) If A = 0, B = 1, and C = 0, then find **X** where $\mathbf{X} = \overline{(A \oplus B)} + C$

(4 marks)

d) Determine the clocked flip-flop described in the following excitation table. x in the table represents a don't care condition.

Qn	Qn+1	Inputs A	Inputs B
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

(7 marks)

e) Identify the clocked flip-flop described in the following characterization table.

Inputs A	Inputs B	Output Qn+1
0	0	Qn
1	0	0
0	1	1
1	1	$\overline{Qn}$

(6 marks)

2. (a) Implement the following switching function on a PAL16L8 device.

$\mathbf{f}(A, B, C, D) = \prod \mathbf{M}(1, 4, 8, 11, 14, 15)$

The logic diagram of PAL16L8 is given in the Appendix. Show the intact PAL fuses by crossing them in the diagram and then attach it to your answer book.

(12 marks)

(b) Implement the minimized form of $\mathbf{f}(A, B, C, D)$ of part (a) by using only 2-input NAND gates.

(6 marks)

(c) Implement the function $\mathbf{f}(A, B, C, D)$ of part (a) by using a suitable size decoder and the minimum number of gates.

(7 marks)

3. (a) Design a 3-bit synchronous counter that has the following sequence: 111, 010, 101, 100, 000 and repeat. The unused states 001, 011, and 110 must always go to (111) state on the NEXT clock pulse. Use negative edge triggered D-type flip-flops.

(9 marks)

(b) Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares. Compare this redesigned counter with the design of part (a).

(16 marks)

4. A combination lock employs a clocked synchronous sequential machine. Design the sequential machine that has an input X and one output, LOCK as shown in Figure Q4. The output LOCK should be 0 if and only if X is 0 and the sequence of inputs received on X at the preceding five clock ticks were 10100.

(a) Draw the state diagram of the sequential machine used in the combination lock.

(10 marks)

(b) Design the sequential machine by employing D flip-flops.

(15 marks)

Figure Q4 is on Page 4

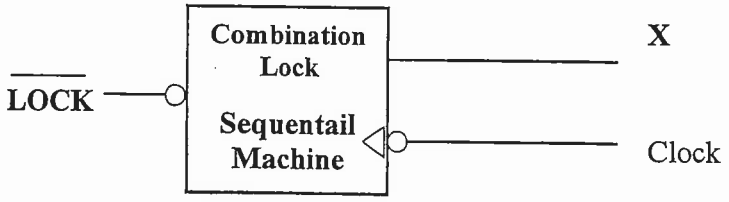


Figure Q4

5. Design and implement a sequential circuit that will serially convert a given 8-bit binary number into its 2's-complement representation. The sequential circuit must satisfy the following conditions:
   - It can have at the most two 8-bit input/output registers, one flip-flop and some logic gates.
   - The conversion of an 8-bit binary number should not take more than 8 clock cycles.

(25 marks)

6. Design a logic circuit required to drive a 7-segment display when driven with a BCD input. Assume that the display requires an active-high input to turn on the LED segment. The seven segments are shown in Figure Q6.

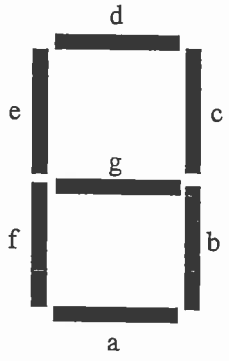


Figure Q6

(a) Construct the truth table and simplify all the output (logic) equations for 7 segments (a, b, c, d, e, f and g).

(12 marks)

Question No. 6 continues on Page 5

(b) Implement the logic circuit using suitable logic gates and draw the logic diagram.

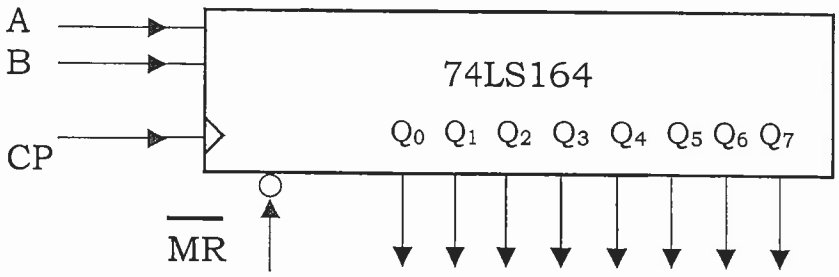
(13 marks)

(END OF QUESTIONS)

APPENDIX

Some Useful Data Sheets

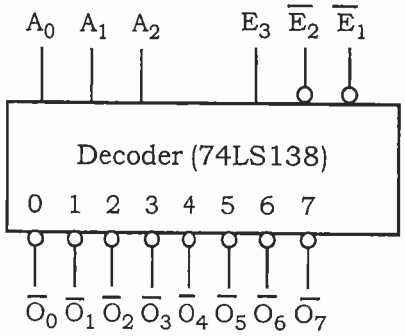
74LS164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0.
- Shift operation occurs at PGTs of the clock input CP.
- The $\overline{MR}$ input resets all FFs asynchronously on a LOW level.

Decoder Data Sheet

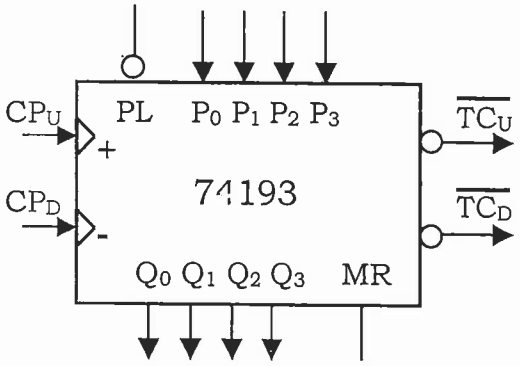
74LS138: 3-to-8 Decoder



Inputs			Outputs
$\overline{E_1}$	$\overline{E_2}$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled - all HIGH
x	1	x	Disabled - all HIGH
x	x	0	Disabled - all HIGH

74193, 4-bit UP/DOWN Counter

MR	$\overline{PL}$	CP_U	CP_D		Mode
H	x	x	x		Asynch Reset
L	L	x	x		Asynch Load
L	H	H	H		No change
L	H	↑	H		Count up
L	H	H	↑		Count down



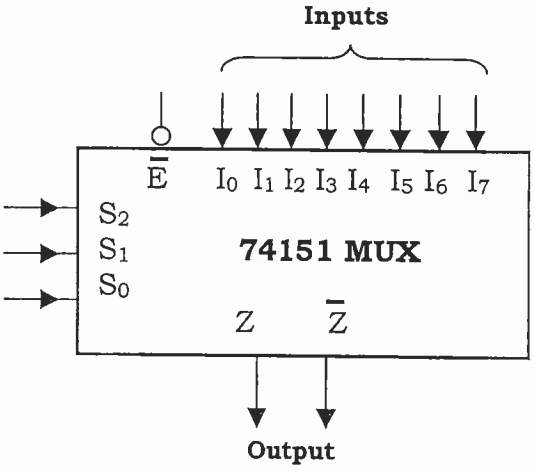
Pins	Description
CP_U	Count-up clock input
CP_D	Count-down clock input
MR	Asynchronous master reset input
$\overline{PL}$	Asynchronous parallel load input
P_0-P_3	Parallel data inputs
Q_0 - Q_3	Flip-flop outputs
$\overline{TC_U}$	Terminal count-up (carry) output
$\overline{TC_D}$	Terminal count-down (borrow) output

Multiplexer Data Sheet

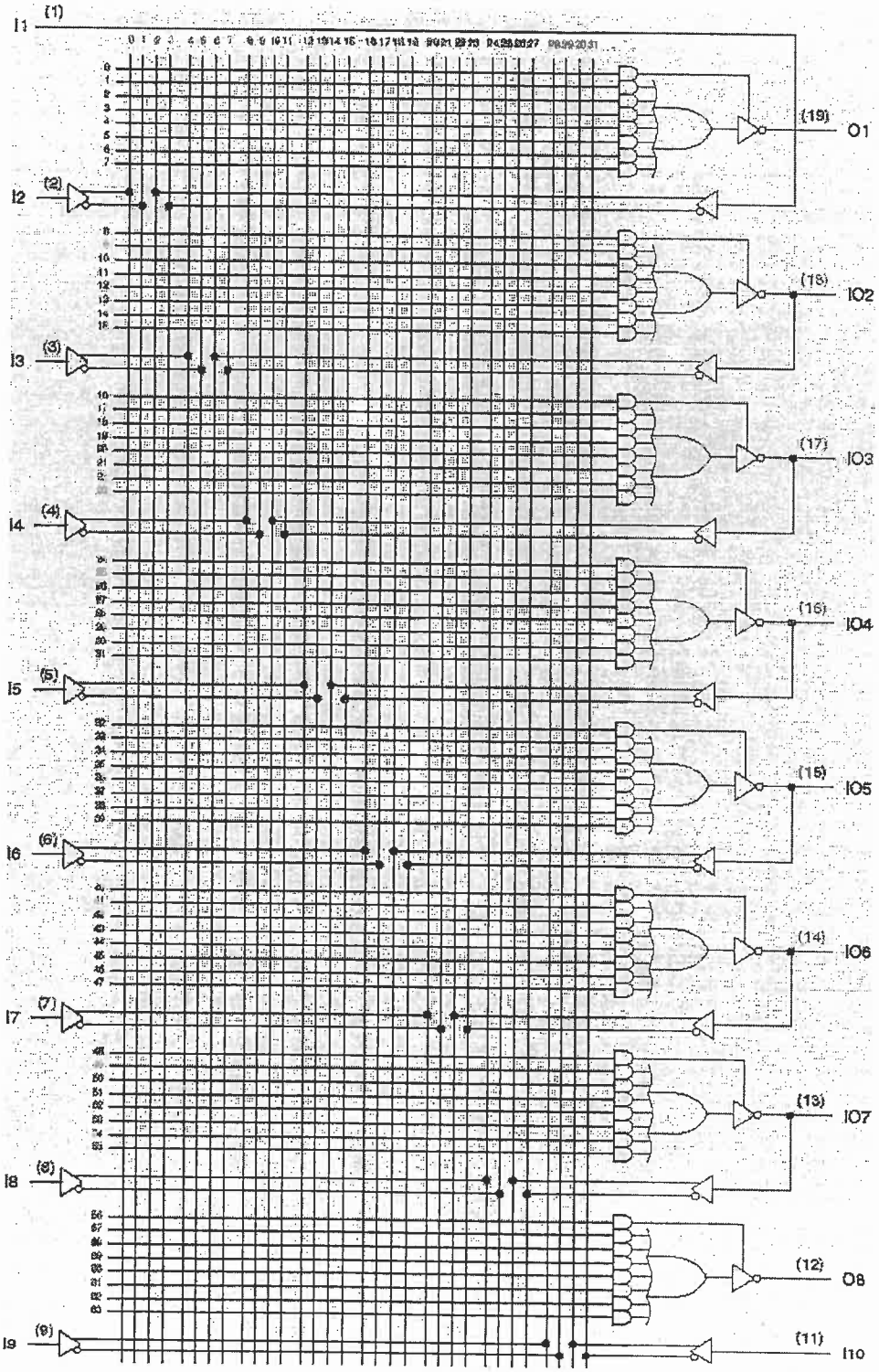
74151 8-to-1 Multiplexer

Inputs Outputs

$\overline{E}$	S_2	S_1	S_0		Z	$\overline{Z}$
H	x	x	x		H	L
L	L	L	L		$\overline{I_0}$	I_0
L	L	L	H		$\overline{I_1}$	I_1
L	L	H	L		$\overline{I_2}$	I_2
L	L	H	H		$\overline{I_3}$	I_3
L	H	L	L		$\overline{I_4}$	I_4
L	H	L	H		$\overline{I_5}$	I_5
L	H	H	L		$\overline{I_6}$	I_6
L	H	H	H		$\overline{I_7}$	I_7



PAL16L8



END OF Paper

Marking Scheme

1. 25 Marks Total
   (a) 6 marks
   (b) 2 marks
   (c) 4 marks
   (d) 7 marks
   (e) 6 marks

2. 25 Marks Total
   (a) 12 marks
   (b) 6 marks
   (c) 7 marks

3. 25 Marks Total
   (a) 9 marks
   (b) 16 marks

4. 25 Marks Total
   (a) 10 marks
   (b) 15 marks

5. 25 Marks

6. 25 Marks Total
   (a) 12 marks
   (b) 13 marks