

National Exams December 2008

07-Elec-B5, Advanced Electronics

3 hours duration

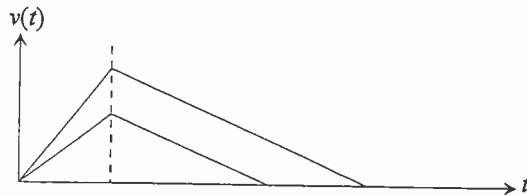
Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a CLOSED BOOK EXAM.
calculator is permitted.
3. Any 5 (FIVE) questions constitute a complete paper. The first five questions as they appear in the answer book will be marked.
4. All questions are worth 20 marks each.
5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are $\pm 15V$.
8. Some questions require an answer in essay format. Clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1)

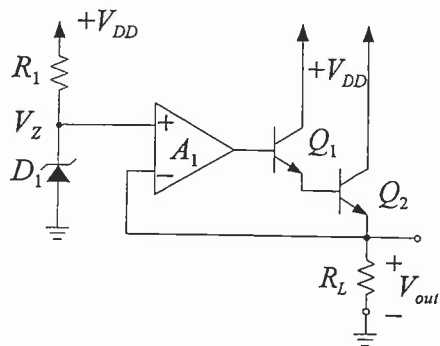
The following voltage waveforms represent the operation of a dual slope Analog to Digital Converters (ADC).

- a) Provide a block level diagram for such type of ADC. Identify all the essential circuit blocks (no detail schematic is required). (8 points)
- b) Provide a brief description on the working principle of dual slope ADC. (8 points)
- c) What are the advantages and disadvantages of dual slope ADCs. What determines the precision? (4 points)



QUESTION (2)

This series voltage regulator has the following components values and device characteristics:



Op amp, A_1 is ideal

$\beta = 100$, $V_{BE} = 0.7 \text{ V}$, $V_T = 25 \text{ mV}$ and $V_A = 100 \text{ V}$ for Q_1

$V_Z = 6.7 \text{ V}$ at $I_Z = 1 \text{ mA}$, $R_Z = 10 \text{ k}\Omega$ for D_1 .

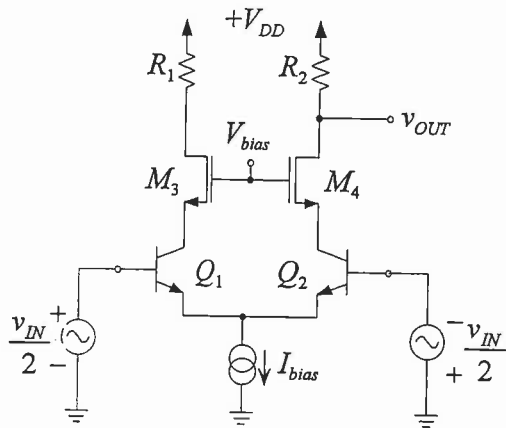
$R_1 = 3.3 \text{ k}\Omega$

$R_L = 4 \Omega$

- a) Given $V_{DD} = 10\text{V}$, what is the nominal output voltage, V_{OUT} ? (4 points)
- b) If V_{DD} has a 1V p-p ripple, what will be the ripple voltage at the output? (8 points)
- c) Find the power efficiency, η of this voltage regulator. (8 points)

QUESTION (3)

In the following circuits, assume all transistors have the following parameters:



$\beta = 100$, $V_{BE} = 0.7 \text{ V}$, $V_T = 25 \text{ mV}$, $V_A = 100 \text{ V}$,
 $K = 0.5 \text{ mA/V}^2$, $V_{TH} = 1 \text{ V}$ and $\lambda = 0.02$.

Given:
 $I_{bias} = 1 \text{ mA}$
 $V_{bias} = 7.5 \text{ V}$
 $V_{DD} = 10 \text{ V}$
 $R_1 = R_2 = 1 \text{ k}\Omega$

- Estimate the differential gain v_{OUT}/v_{IN} in (V/V). (6 points)
- Find the common mode input resistance R_{icm} . (4 points)
- Find the common mode input range. (4 points)
- Estimate the common mode rejection ratio, CMRR. Express your result in dB. (6 points)

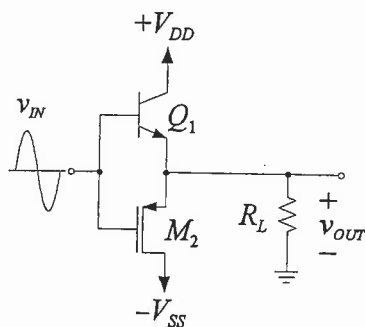
Useful formulae: for n-channel MOSFET

$$i_{DS} = K \left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2 \right] \quad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K (v_{GS} - V_{TH})^2 (1 + \lambda v_{DS}) \quad \text{saturation region}$$

QUESTION (4)

The following is a class B output stage.

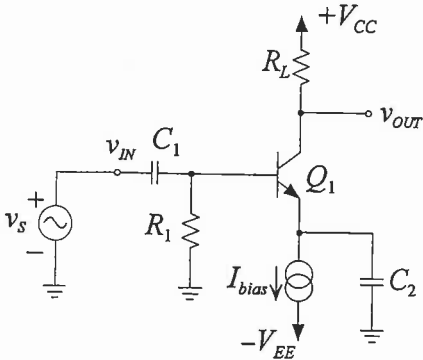


Given: $\beta = 100$, $V_{BE} = 0.7 \text{ V}$, $V_{CE(sat)} = 0.3 \text{ V}$, $V_T = 25 \text{ mV}$,
 $V_A = 100 \text{ V}$,
 $K = 500 \text{ mA/V}^2$, $V_{TH} = 1.0 \text{ V}$,
 $R_L = 8 \Omega$ and $|V_{DD}| = |V_{SS}| = 10 \text{ V}$.

- The maximum RMS output power. (4 points)
- The RMS power dissipated by M1 under maximum output power. (8 points)
- The power efficiency, η of this output stage. (8 points)

QUESTION (5)

In the following circuit, assume that $\beta = 100$, $V_{BE} = 0.7 \text{ V}$, $V_{CE(sat)} = 0.3 \text{ V}$, $V_A = 100 \text{ V}$, $C_{\mu} = 2 \text{ pF}$ for all transistors. Neglect r_x and r_o in the hybrid- π model.

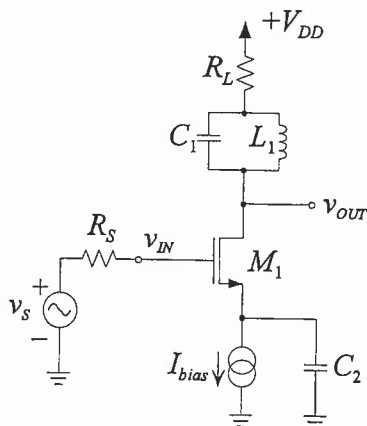


- Given: $R_L = 5 \text{ k}\Omega$
 $R_1 = 1 \text{ k}\Omega$
 $C_1 = 10 \text{ }\mu\text{F}$
 $C_2 = \infty$
 $|V_{CC}| = |V_{EE}| = 10 \text{ V}$
 $I_{bias} = 1 \text{ mA}$
 $V_T = 25 \text{ mV}$

- Estimate the mid-band gain v_{OUT}/v_S in (V/V). (4 points)
- Find the lower 3dB frequency f_L in (Hz). (4 points)
- Find the upper 3dB frequency f_H in (Hz). (6 points)
- Find the 2nd high frequency dominant pole in (Hz). (6 points)

QUESTION (6)

In the following tuned amplifier circuit, the transistor M_1 is biased such that $V_{DD} = 10 \text{ V}$, $I_{bias} = 2 \text{ mA}$. The transistor parameters are given as $K = 1 \text{ mA/V}^2$, $V_{TH} = 1 \text{ V}$, $C_{gs} = 10 \text{ pF}$, $C_{gd} = 1 \text{ pF}$, and $\lambda = 0$.



- For: $L_1 = 1 \text{ }\mu\text{H}$
 $C_1 = 200 \text{ pF}$, $C_2 = \infty$
 $R_S = 1 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$

- What is the center frequency, ω_o of this amplifier? (4 points)
- What is the gain v_{OUT}/v_S at $\omega = \omega_o$? (8 points)
- What is the 3dB bandwidth of this tuned amplifier? (8 points)

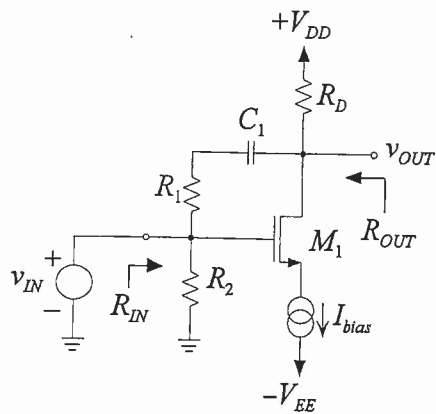
Useful formulae: for n-channel MOSFET

$$i_{DS} = K \left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2 \right] \quad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K (v_{GS} - V_{TH})^2 (1 + \lambda v_{DS}) \quad \text{saturation region}$$

QUESTION (7)

Consider the following amplifier with a feedback circuit.



Given: $R_D = 3\text{ k}\Omega$, $C_1 = \infty$, $R_2 = 20\text{ k}\Omega$

$|V_{CC}| = |V_{EE}| = 10\text{ V}$

$I_{bias} = 1\text{ mA}$

$K = 1\text{ mA/V}^2$, $V_{TH} = 1\text{ V}$, and $\lambda = 0$

- Determine the input and output resistance (R_{IN} and R_{OUT}) if there is no feedback network (i.e. $R_1 = \infty$). (8 points)
- Determine the input and output resistance (R_{IN} and R_{OUT}) if $R_1 = 100\text{ k}\Omega$. (12 points)