National Exams – December 2009

07-Elec-A4, Digital Systems & Computers

3 Hours Duration

NOTES

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made;

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a Closed Book exam.

3. Any five questions constitute a complete paper. Only the first five questions as they appear in your answer book will be marked.

4. All questions are of equal value

Marking Scheme:

1. (a) 2, (b) 4, (c) 10, (d) 4
2. (a) 4, (b) 8, (c) 8
3. 20
4. 20
5. (a) 6, (b) 6, (c) 8
6. 20

1.

Considering the Karnaugh map shown below for variables A, B, C and D.

a) Draw the Truth Table which the K map represents.
b) Write the min term expression f (A, B, C, D) = ∑m ( ).
c) Write the logical function derived from the K-map, and
d) Draw the logic gate architecture, which realizes the logical function obtained in c).

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CD \ AB	00	01	11	10
00	0: 1	4: 0	12: 1	8: 0
01	1: 1	5: 1	13: 1	9: 1
11	3: 1	7: 0	15: 1	11: 1
10	2: 0	6: 1	14: 0	10: 0

2.

Considering the sequential circuit below:

a) Determine the input functions to each JK flip-flop in terms of A, B, and x.
b) Construct the state table for the sequential circuit.
c) Draw and label the state diagram for the sequential circuit.

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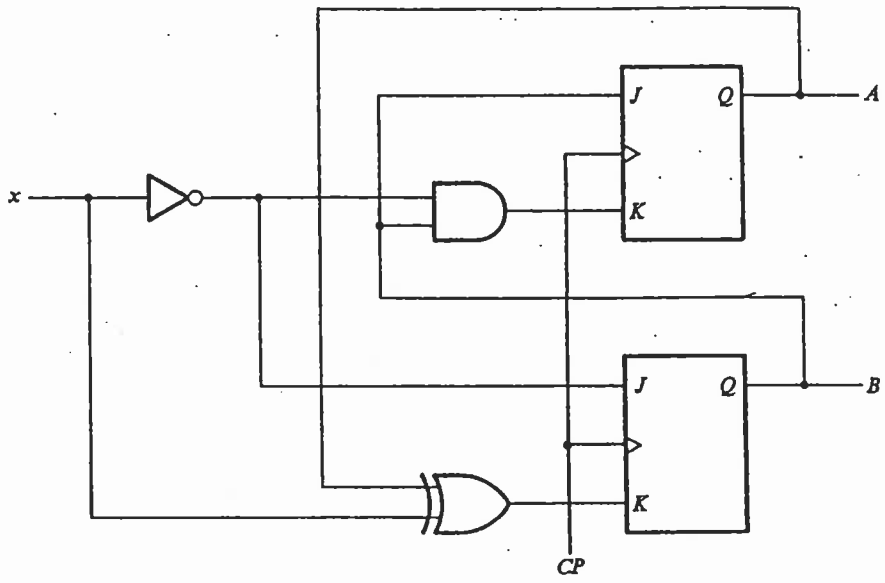

3.

The following is a state table for a sequential circuit which has a number of unused states. Draw the logic diagram of the **minimum** sequential circuit which implements the truth table. Your answers should include:

a) K-maps for SA, SB, SC, RA, RB, RC, and Y
b) Logical functions for SA, SB, SC, RA, RB, RC, and y
c) The designed circuit.

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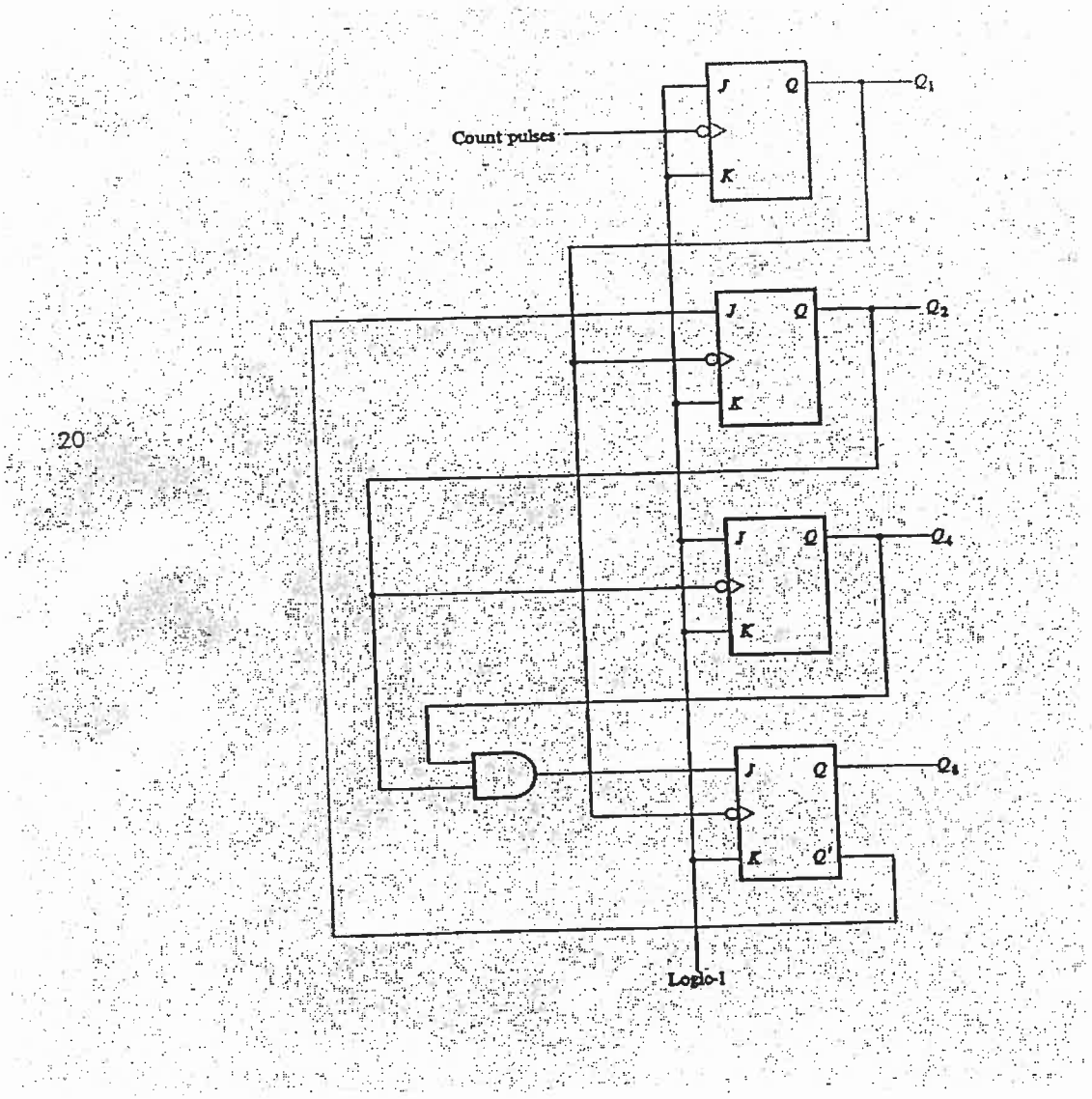
Present State	Input	Next State	Flip-Flop Inputs						Output
A B C	x	A B C	SA	RA	SB	RB	SC	RC	y
0 0 1	0	0 0 1	0	X	0	X	X	0	0
0 0 1	1	0 1 0	0	X	1	0	0	1	0
0 1 0	0	0 1 1	0	X	X	0	1	0	0
0 1 0	1	1 0 0	1	0	0	1	0	X	0
0 1 1	0	0 0 1	0	X	0	1	X	0	0
0 1 1	1	1 0 0	1	0	0	1	0	1	0
1 0 0	0	1 0 1	X	0	0	X	1	0	0
1 0 0	1	1 0 0	X	0	0	X	0	X	1
1 0 1	0	0 0 1	0	1	0	X	X	0	0
1 0 1	1	1 0 0	X	0	0	X	0	1	1

4.

Identify the following logic circuit by constructing a truth table and/or timing diagram to display the states of Q_1 to Q_8 when the circuit is clocked with sixteen clock pulses. Assume that the JK flip-flops are triggered on the negative or trailing edge of the clock pulse.



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5.

a) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
b) How many lines of the address must be used to access 2048 bytes? How many of these lines are connected to the address inputs of all chips?
c) How many lines must be decoded for the chip-select inputs? Specify the size of the decoder.

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6.

The following is the basic architecture of a computer. Construct a table which has three headings: Clock Cycle, Micro Operation, and Explanation. For each clock cycle give the micro operations necessary to call a subroutine stored in memory. This is the CSR instruction. For each micro operation provide an explanation of the transfer or interchange of addresses or contents of the memory, registers, etc.

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