National Exams – May 2009

07-Elec-A4, Digital Systems and Computers

3 Hours Duration

NOTES

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made;
2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a Closed Book exam.
3. Any five questions constitute a complete paper. Only the first five questions as they appear in your answer book will be marked.
4. All questions are of equal value

1. Provide the minimum form of the following Boolean function using a five variable K-map.

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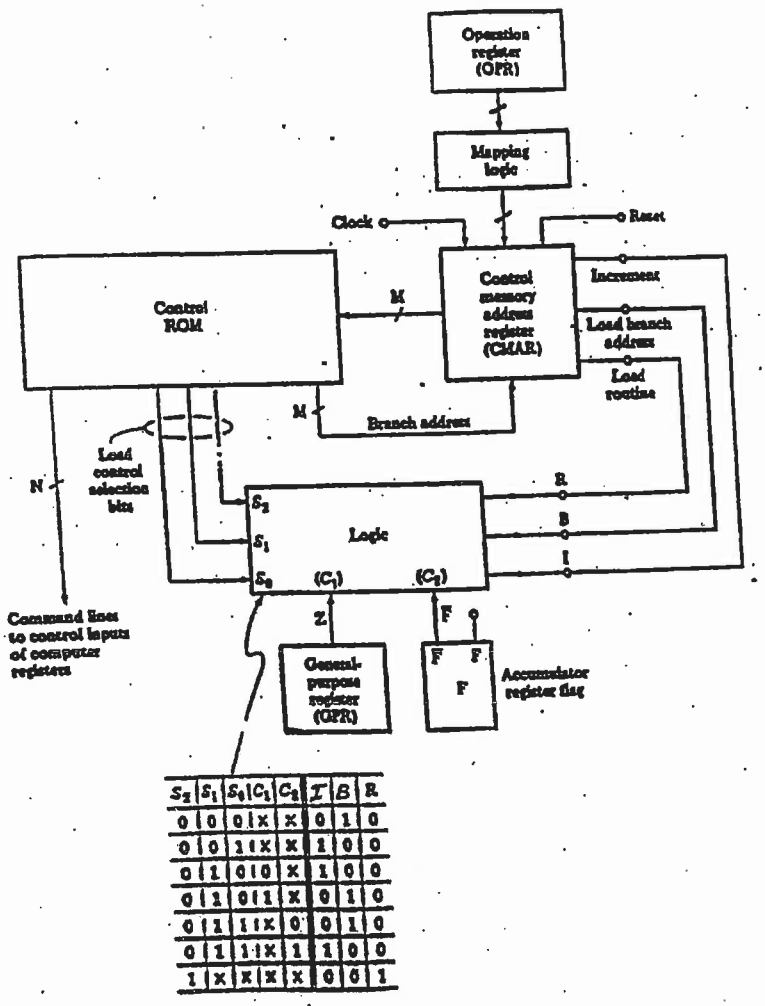
$$F = \bar{A}\,\bar{B}\,C\,\bar{E} + \bar{A}\,\bar{B}\,\bar{C}\,\bar{D} + \bar{B}\,\bar{D}\,\bar{E} + \bar{B}\,C\,\bar{D} + C\,D\,\bar{E} + B\,D\,\bar{E}$$

The box numbering for a five variable K-map is on an attached sheet.

2. Design a sequential circuit with two JK flip-flops, A and B, and two inputs, E and x. If E = 0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through state transitions from 00 to 11 to 10 to 01 back to 00, and repeats. Your answer should include: **20**

   a) K-maps for JA, JB, KA, KB
   b) Logical functions for JA, JB, KA, KB
   c) The diagram of the sequential circuit which represents the design.

3. The following architecture represents a ROM controller for a microcomputer. The logic box in the controller with inputs S_2, S_1, and S_0 (load control section bits) and C_1, C_2 (status bits), has to be designed using combinational logic gates. Considering that the truth tables for this logic box is given at the bottom of the circuit, draw the minimum circuit necessary to implement the truth table. **20**



S_2	S_1	S_0	C_1	C_2	I	B	R
0	0	0	x	x	0	1	0
0	0	1	x	x	1	0	0
0	1	0	0	x	1	0	0
0	1	0	1	x	0	1	0
0	1	1	x	0	0	1	0
0	1	1	x	1	1	0	0
1	x	x	x	x	0	0	1

4. The following is a state table for a sequential circuit which has a number of unused states. Draw the logic diagram of the minimum sequential circuit which implements the truth table. Your answers should include:

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a) K-maps for SA, SB, SC, RA, RB, RC, and Y
b) Logical functions for SA, SB, SC, RA, RB, RC, and y
c) The designed circuit.

Present State	Input	Next State	Flip-Flop Inputs						Output
A B C	x	A B C	SA	RA	SB	RB	SC	RC	y
0 0 1	0	0 0 1	0	X	0	X	X	0	0
0 0 1	1	0 1 0	0	X	1	0	0	1	0
0 1 0	0	0 1 1	0	X	X	0	1	0	0
0 1 0	1	1 0 0	1	0	0	1	0	X	0
0 1 1	0	0 0 1	0	X	0	1	X	0	0
0 1 1	1	1 0 0	1	0	0	1	0	1	0
1 0 0	0	1 0 1	X	0	0	X	1	0	0
1 0 0	1	1 0 0	X	0	0	X	0	X	1
1 0 1	0	0 0 1	0	1	0	X	X	0	0
1 0 1	1	1 0 0	X	0	0	X	0	1	1

5. Identify the following logic circuit by constructing a truth table and/or timing diagram to display the states of Q_1 to Q_8 when the circuit is clocked with sixteen clock pulses. Assume that the JK flip-flops are triggered on the negative or trailing edge of the clock pulse.

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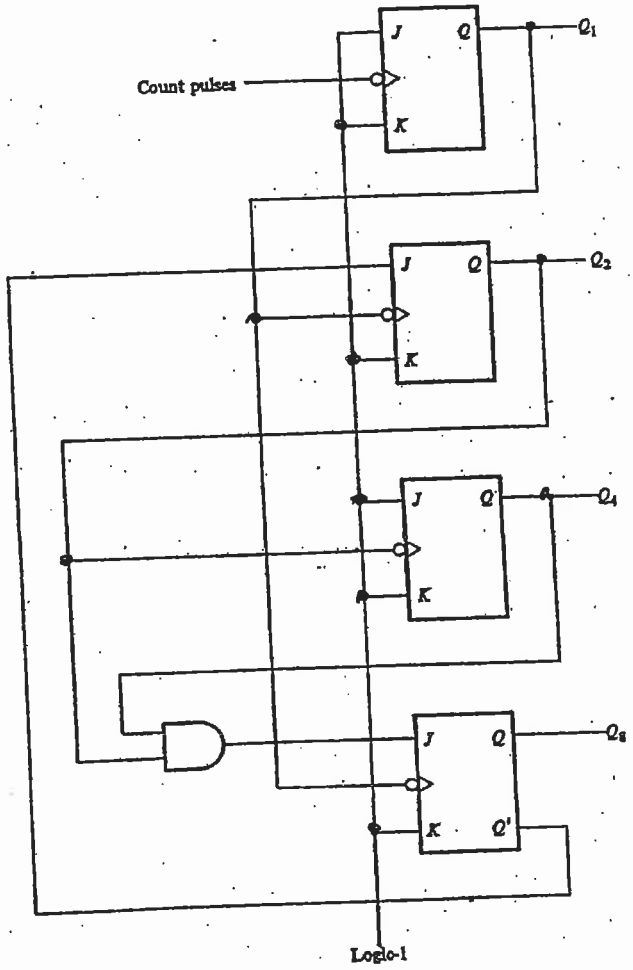

6. a) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
   b) How many lines of the address must be used to access 2048 bytes? How many of these lines are connected to the address inputs of all chips?
   c) How many lines must be decoded for the chip-select inputs? Specify the size of the decoder.

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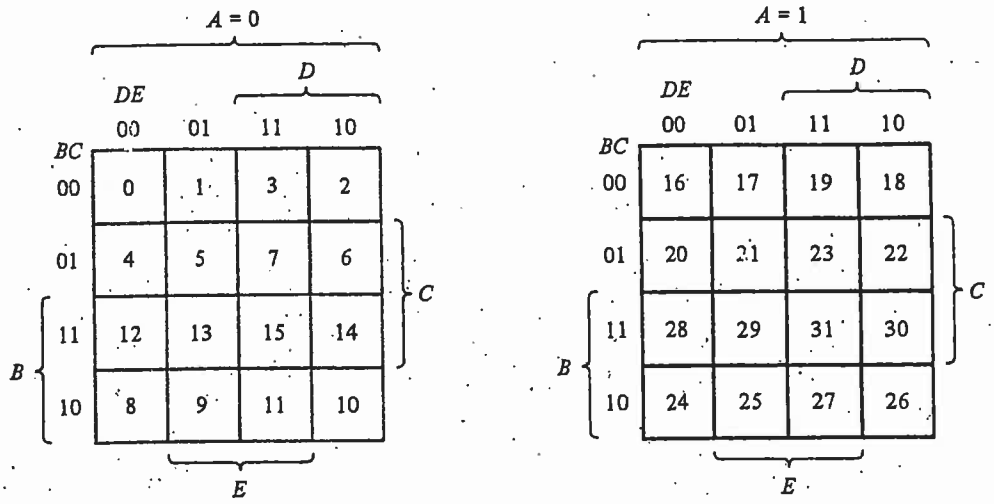

FIGURE 3-12
Five-variable map

Marking Scheme:

1. 20
2. (a) 8, (b) 8, (c) 4
3. 20
4. (a) 6, (b) 6, (c) 8
5. 20
6. (a) 4, (b) 8, (c) 8