National Exams May 2010

07-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. All FIVE (5) questions constitute a complete exam paper.

4. All questions are of equal value.

Marking Scheme

1. (a) 3, (b) 3, (c) 3, (d) 3
2. (a) 3, (b) 6, (c) 3
3. (a) 6, (b) 3, (c) 3
4. (a) 6, (b) 6
5. (a) 5, (b) 7

The number beside each part above indicates the points that part is worth

1.- Given the following function in product-of-sums (PoS) form:

$$f(A,B,C,D) = (B+\overline{C})\cdot(\overline{A}+\overline{B}+C)\cdot(B+C+D)$$

(a) Prepare its truth table.   [3 pts]

(b) Express f in canonical sum of products (SoP) form using the abbreviated notation
   involving minterms, i.e., $f(A,B,C,D) = \sum m_i (\ldots)$ [3 pts]

(c) Map the function f in a Karnaugh map (K-map) and find the minimized SoP form.   [3 pts]

Note: Alternatively you can verify this result using Boolean algebra, a summary of
      identities is provided in a table attached at the end.

(d) Is the expression found in part (c) hazard-free? If not, give the hazard-free SoP form.   [3 pts]

2.-   The following circuit contains two JK flip-flops.

    (a)   Write the logic expressions for J_A, K_A, J_B and K_B.   [3 pts]

    (b)   Obtain the state transition table for the circuit.   [6 pts]

    (c)   Sketch the state transition diagram for the circuit.   [3 pts]
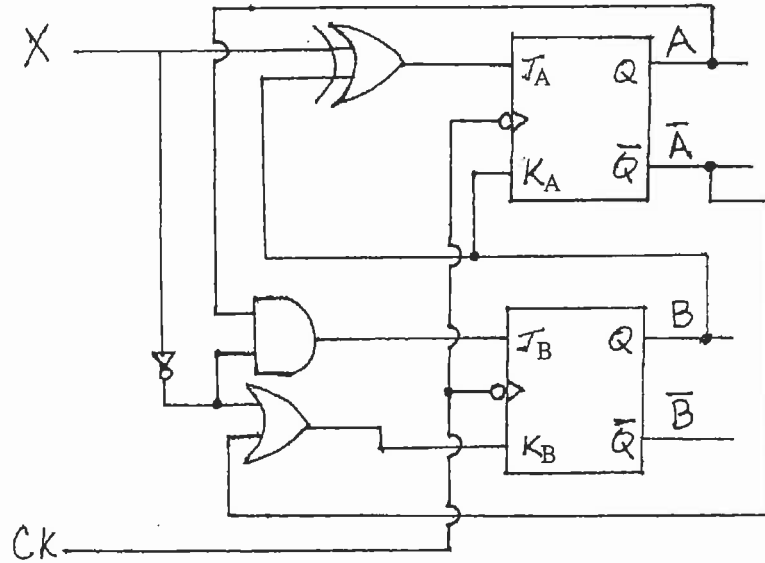
Note: Consult the flip-flop excitation table attached at the end as needed.

3.-   A 3-bit counter advances through the sequence 001, 011, 010, 100, 111 back to 001 and repeats.

   (a) Using the standard design process for synchronous counters, show how to implement this counter using D flip-flops. Include:

      – state transition diagram,

      – state transition table, and

      – a drawing of the final circuit implementing the counter.   [6 pts]

   (b) Check whether the counter is self-starting or not.   [3 pts]

   (c) Sketch the timing diagram for the counter showing its dynamic behavior, include:

      - The clock waveform CLK, and

      - The output waveforms Q_A, Q_B & Q_C, where Q_A is the output of flip-flop A, Q_B is the output of flip-flop B and Q_C is the output of flip-flop C.

      Assume the $\overline{\text{CLR}}$ input of all flip-flops is temporarily held LOW during the clock cycles preceding time $t = 0$.   [3 pts]

4.- (a) Describe the algorithm of a short assembly program, including any additional routines needed, in charge of   [6 pts]

1. Reading ONE (1) character (char) received through an asynchronous serial port,
2. Converting that char received to lowercase if uppercase, or viceversa (assume the char received is a letter), and
3. Transmitting the char obtained in Step 2 above through the asynchronous serial port using interrupts.

You can use a subroutine called inchar starting at address $FFCD_{hex}$. This subroutine loops until a character is received by the input serial port then returns the ASCII character in a CPU register called accumulator A (ACCA).

Assume the asynchronous serial port has been initialized already including a serial line speed of 9600 baud.

Assume standard serial port registers: status (SR), control (CR), transmit data (TDR) and receive data (RDR) are memory mapped and their addresses available.

(b) Both input and output serial channels support RS-232 levels, this is, the microprocessor board receive data (RxD) line is coupled to the channel through RS-232 receivers and the transmit data (TxD) line is coupled to the channel through RS-232 drivers.

Assume the character 'U' is received by your program through the serial port.

Once your program runs sketch the time waveforms for:

(i) the serial bit stream on the TxD line in the board before the RS-232 drivers, and

(ii) the same serial bit stream in (i) above on the transmit line of the RS-232 cable connected to the board serial port connector.

Label each bit appropriately according to their position and role in the frame.

Include time scale values and voltage scale values for each case.   [6 pts]

Assume CMOS logic levels are used within the microprocessor board.

ASCII value for 'U' is 55_{hex}

ASCII value for 'u' is 75_{hex}

hex stands for hexadecimal

5.- Two new external memory chips need to be added to a microprocessor system – a 4Kbyte RAM that should begin at $8800, and a 2Kbyte EPROM that should begin at $B800. Regions $9800-$9FFF, $B600-$B7FF & $C000-$FFFF of the memory map are in use already and conflict should be avoided.

(a) Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers. The number on top of this symbol ⟶╱⟶ represents the number of lines on that bus.   [5 pts]

(b) $\overline{E_1}$ & $\overline{E_2}$ are the active-low chip select pins for the RAM & EPROM chips, respectively. Find their Boolean expressions. Use the minimum number of lines and gates possible. Use decoder outputs to minimize decoding logic. Complete the connections in the figure below (adding logic gates where needed) to create the address decoding specified.   [7 pts]

Note: The '$' sign indicates the number following it is a hexadecimal number.
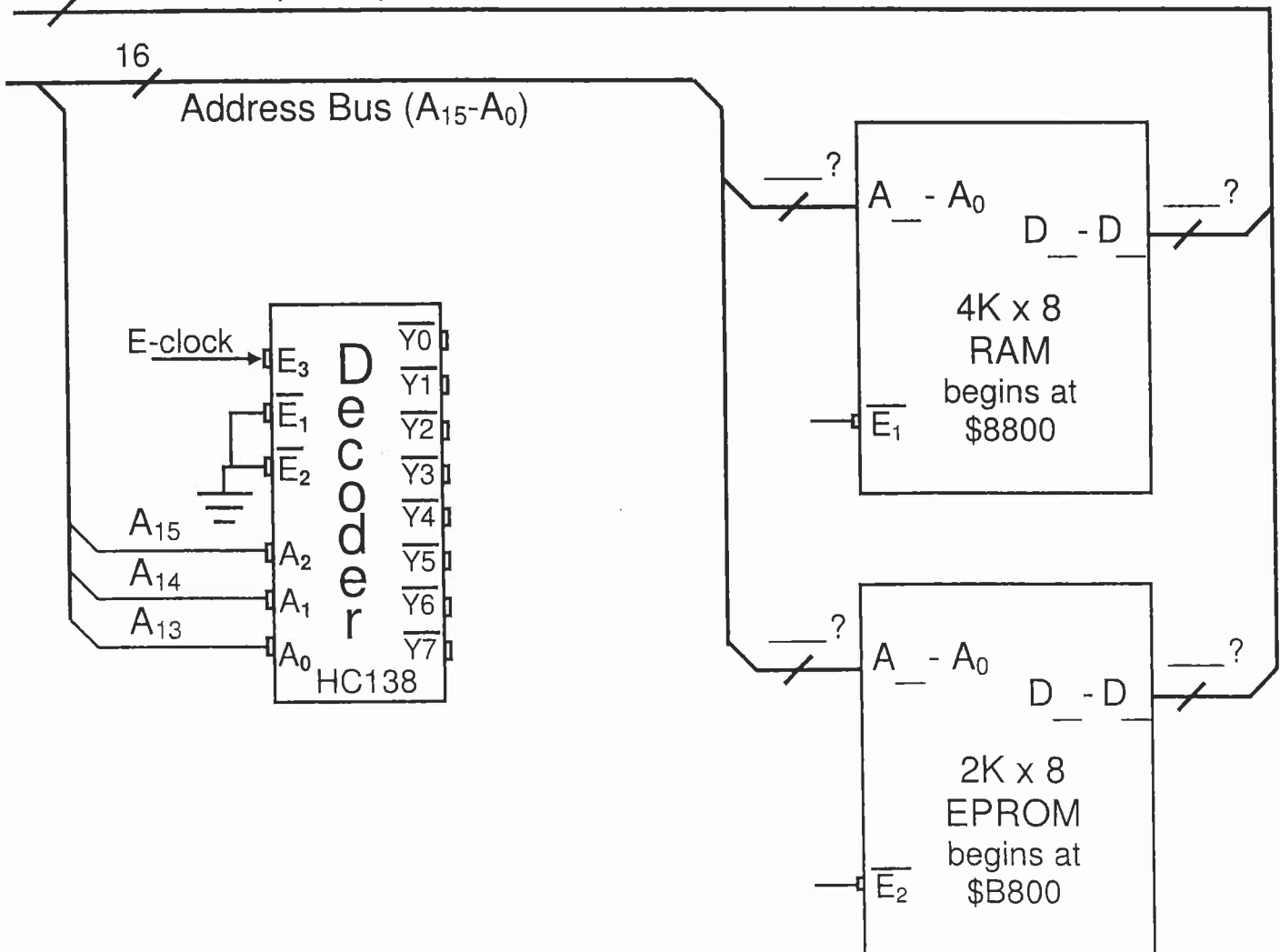
Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A + 0 = A$	Operations with 0 and 1
2.	$A + 1 = 1$	Operations with 0 and 1
3.	$A + A = A$	Idompotent
4.	$A + \overline{A} = 1$	Complementarity
5.	$A \cdot 0 = 0$	Operations with 0 and 1
6.	$A \cdot 1 = A$	Operations with 0 and 1
7.	$A \cdot A = A$	Idompotent
8.	$A \cdot \overline{A} = 0$	Complementarity
9.	$\overline{\overline{A}} = A$	Involution
10.	$A + B = B + A$	Commutative
11.	$A \cdot B = B \cdot A$	Commutative
12.	$A + (B + C) = (A + B) + C = A + B + C$	Associative
13.	$A \cdot (B \cdot C) = (A \cdot B) \cdot C = A \cdot B \cdot C$	Associative
14.	$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$	Distributive
15.	$A + (B \cdot C) = (A + B) \cdot (A + C)$	Distributive
16.	$A + (A \cdot B) = A$	Absorption
17.	$A \cdot (A + B) = A$	Absorption
18.	$(A \cdot B) + (\overline{A} \cdot C) + (B \cdot C) = (A \cdot B) + (\overline{A} \cdot C)$	Consensus
19.	$\overline{A + B + C + \ldots} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \ldots$	De Morgan
20.	$\overline{A \cdot B \cdot C \cdot \ldots} = \overline{A} + \overline{B} + \overline{C} + \ldots$	De Morgan
21.	$(A + \overline{B}) \cdot B = A \cdot B$	Simplification
22.	$(A \cdot \overline{B}) + B = A + B$	Simplification