National Exams November/December 2011

07-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 2, (b) 2, (c) 2, (d) 2, (e) 2, (f) 2, total = 12
2. (a) 6, (b) 3, (c) 3, total = 12
3. (a) 2.5, (b) 4.5, (c) 3, (d) 2, total = 12
4. (a) 2.5, (b) 2.5, (c) 2.5, (d) 4.5, total = 12
5. (a) 4, (b) 4, (c) 4, total = 12
6. (a) 2, (b) 2, (c) i. 3, (c) ii. 3, (c) iii. 2, total = 12

The number beside each part above indicates the points that part is worth

1.- Given the following function in sum-of-products form:

$$f(A,B,C) = \overline{A}\cdot B\cdot\overline{C} + \overline{A}\cdot\overline{B} + \overline{B}\cdot C + A\cdot\overline{B}\cdot\overline{C}$$

(a) Prepare its truth table.

(b) Express f in canonical product-of-sums form.

(c) Express f in minimized product-of-sums form (*Hint*: Use the K-map approach).

(d) Express f in minimized sum-of-products form.

(e) Synthesize a NOR-only circuit for f using a minimum number of gates.

(f) Synthesize a NAND-only circuit for f using a minimum number of gates.

2.- A 3-bit counter advances through the sequence 000, 001, 011, 101, 110, 111 back to 000 and repeats.

(a) Using the standard design process for synchronous counters, show how to implement this counter using JK flip-flops. Include:

– state transition diagram,

– state transition table including flip-flop inputs, and

– a drawing of the final circuit implementing the counter.

(b) Check whether the counter is self-starting or not.

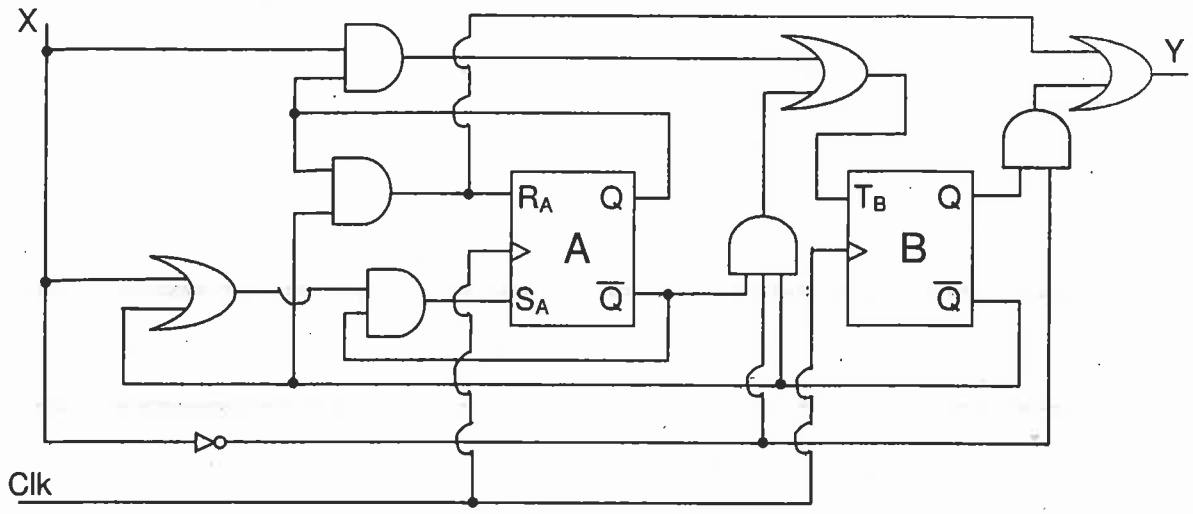
(c) Sketch the timing diagram for the counter showing its dynamic behavior, include:

- The clock waveform CLK, containing at least six clock pulses after $t = 0$, and
- The output waveforms Q_A, Q_B & Q_C, where Q_A is the output of flip-flop A (MSB[1]), Q_B is the output of flip-flop B and Q_C is the output of flip-flop C (LSB[1]).

Assume the $\overline{CLR}$ input of all flip-flops is temporarily held LOW during the clock cycles preceding time $t = 0$.

[1] MSB: most significant bit, LSB: least significant bit

3.- The following circuit with input X and output Y uses one RS flip-flop and a T flip-flop.



(a) Write the logic expressions for R_A, S_A, T_B and Y.

(b) Obtain the state transition table for the circuit.

(c) Sketch the state transition diagram for the circuit.

(d) Is this a Moore or a Mealy machine? Explain.

Note: Consult flip-flop excitation tables attached at the end as needed.

4.- (a) There are two techniques in a computer system for peripheral interfaces to communicate with the processor or CPU; these are polling and interrupts.
Describe the difference between the polling and the interrupt methods.
Explain which one is more efficient and why?

(b) Explain the difference between synchronous and asynchronous serial communication.
Mention the factors that make asynchronous serial communication possible.

(c) Where is the use of parallel-to-serial shift registers needed, in the receiving unit of a serial comm port or in its transmitting unit? Explain.

(d) The figure next page shows an external serial communication interface. All three chip select inputs (CS_0, CS_1 & CS_2) need to be at their active levels in order for the interface chip to be enabled.
The table below shows how the $R/\overline{W}$ & RS input signals are used to access the registers of the interface chip.

Knowing that the TDRE[(1)] flag is bit 1 of the status register and that the chip has been programmed for transmission without interrupts. Describe the algorithm for an assembly program that:

i. Checks when the interface chip is ready to accept a new data byte from the CPU for transmission, then
ii. Sends the byte to the interface chip for transmission.

Be specific as to which addresses need to be used to access the interface registers needed and the bitmask needed to check the right flag.

(1) Transmit Data Register Empty

In the decoder: output $\overline{Y0}$ is active when inputs $A_2A_1A_0 = 000$,
output $\overline{Y1}$ is active when inputs $A_2A_1A_0 = 001$,
output $\overline{Y2}$ is active when inputs $A_2A_1A_0 = 010$, and so on...

Register Select Input (RS)	$R/\overline{W}$	Register Selected
1	0	Tx Data Register (TDR)
1	1	Rx Data Register (RDR)
0	0	Control Register (CR)
0	1	Status Register (SR)

Table.- Interface register selection.

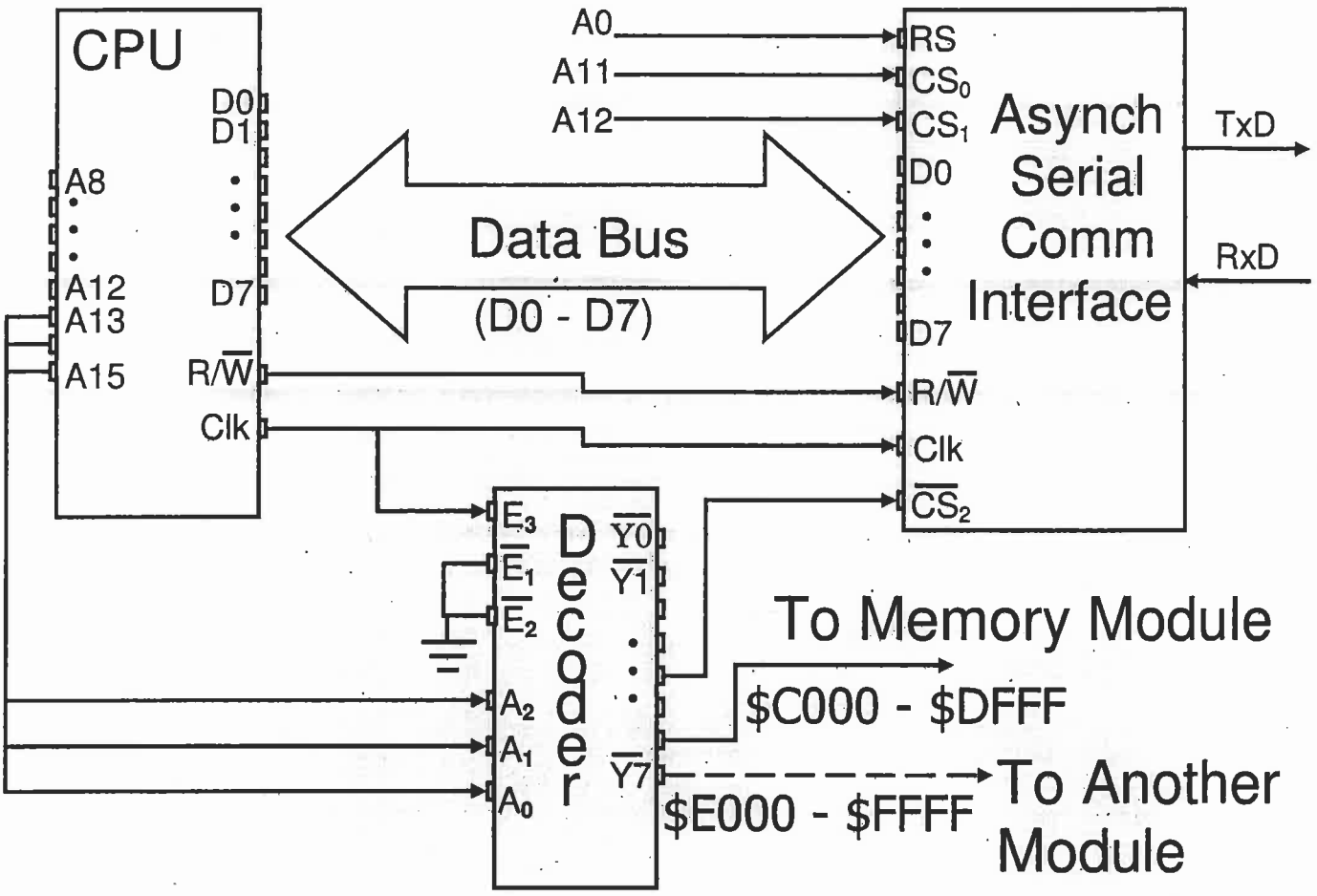


Figure.- Connections to the external Asynchronous Serial Comm Interface

5.- (a) Identify by marking with a X which of the following are the 4 essential components of a computer system.

__ Mouse
__ Busses (address, data, control)
__ Processor (CPU)
__ Keyboard
__ Printer
__ Display monitor
__ Hard drive
__ I/O ports
__ Memory

(b) Mention the main differences between a general purpose microprocessor and a microcontroller.

(c) Mention which CPU register(s) is(are) typically associated with each of the following

- the address of the next instruction to be executed : _____
- the next available location at the top of the stack : _____
- pointing to an array or list of data values in memory : _____
- containing the information an assembly program uses at decision making points (conditional branch statements): _____

6.- (a) Mention two differences between the address bus and the data bus of a computer system.

(b) A microprocessor system has an address bus with 16 lines, A_{15}-A_0, and a data bus with 8 lines, D_7-D_0. What is the memory space of the system (in Kbyte)? Justify. Indicate the address range of the entire memory space providing the lowest and highest addresses.

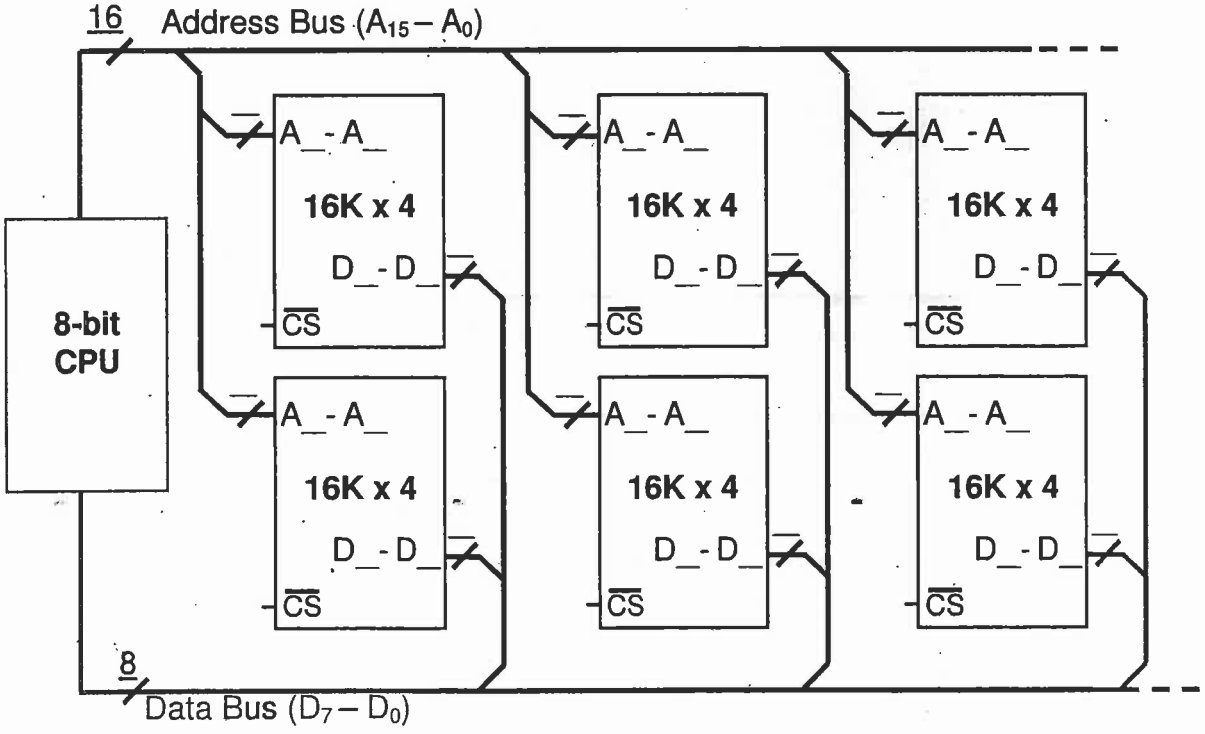
(c) Provide the 8-bit CPU in the figure below with a 48Kbyte memory space by making use of 16K x 4 memory chips like the ones provided in the figure below.

i. Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers. The number on top of this symbol ⟋ represents the number of lines on that bus. The spaces besides the A's and the D's indicate which set of lines of the address or data bus is connected to each chip, respectively.

ii. Complete the connections in the figure below adding logic gates where needed to produce the chip select (CS) signals needed (the decoding logic). Explain the reasons for the connections made; include expressions for the Boolean logic used.

iii. Provide the address range allocated to each chip.

Note: R/$\overline{W}$ & clock signals are omitted for simplicity.



Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot\overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification