

National Exams December 2011

07-Elec-B6 – Integrated Circuit Engineering

3 Hours Duration

Notes:

If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made.

Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book exam.

Any five questions constitute a complete paper. Only the first five questions as they appear in your answer book will be marked.

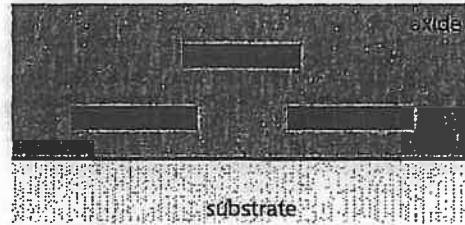
All questions are of equal value. Marks for individual parts of questions are listed where appropriate.

*n*-channel MOSFET drain current equations (*p*-channel similar with the usual sign and variable changes)

$$I_D = \frac{W}{L} \bar{\mu}_n \hat{C}_{ox} \left( (V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right) \text{ triode}$$
$$= \frac{W}{L} \bar{\mu}_p \hat{C}_{ox} \frac{(V_{GS} - V_{Th})^2}{2} \text{ saturation}$$

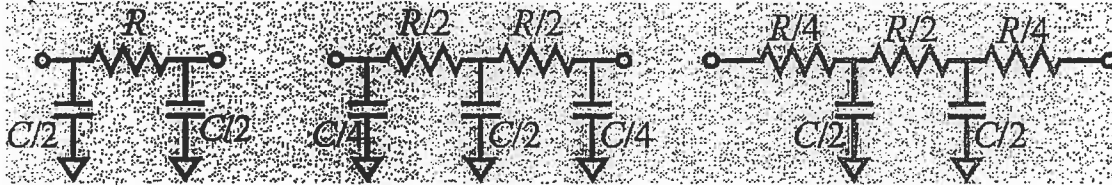
**Question 1. (Total 20 marks)**

a) (6 marks) For an interconnect structure consisting of three metal lines running above the surface of a substrate that can be considered conductive, as shown in cross-section in the diagram to the right, identify all components of capacitance. Reproduce the diagram in your answer book and indicate field lines to identify capacitances.

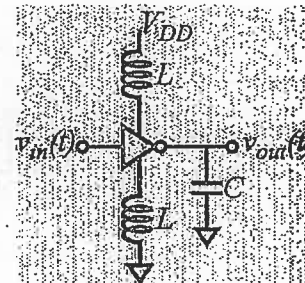


b) (4 marks) When is a distributed model necessary for an interconnect line, and why?

c) (4 marks) Using the Elmore delay model, find the time constant of each RC delay line equivalent circuit shown below.



d) (6 marks) The circuit to the right shows a CMOS inverter driving a capacitive load with inductances simulating the effect of bondwires in the power supply path. If  $V_{DD} = 5\text{ V}$ ,  $C = 10\text{ pF}$  and  $L = 5\text{ nH}$ , estimate the change in power supply voltage during a step function input from 0 to  $V_{DD}$ . Assume the charging current increases and decreases linearly over a 10-90% switching period of 3 nsec (i.e. a triangular distribution), with a peak value such that the linear distribution has the same average value as the average current over the switching time.



**Question 2 (Total 20 marks)**

Show the processing steps necessary to fabricate a high-quality vertical npn bipolar transistor starting from the bare surface of a p-type substrate wafer. Clearly depict the role of masks in the process flow. The complete structure should include metal contacts to the emitter, base and collector. Use a series of cross-sections showing development of the structure and layers.

**Question 3 (Total 20 marks)**

Consider a simple CMOS inverter with n-channel parameters  $V_{Tn}$ ,  $\mu_n$ ,  $W_n$  and  $L_n$ , and p-channel parameters  $V_{Tp}$ ,  $\mu_p$ ,  $W_p$  and  $L_p$ . Assume  $|V_{Tp}| = V_{Tn}$ .

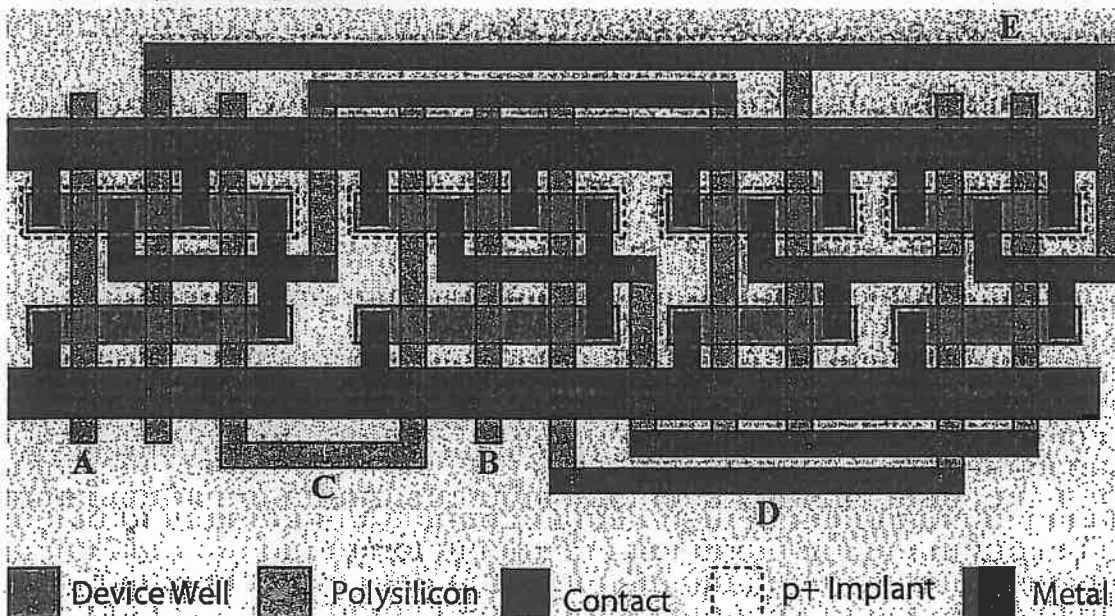
a) (5 marks) Derive an expression for the inverter threshold.

- b) (5 marks) Sketch the static transfer characteristic of the gate assuming an inverter threshold of  $V_{DD}/2$ . Define the quantities  $V_{IL}$ ,  $V_{OL}$ ,  $V_{IH}$  and  $V_{OH}$  and show their positions on the static transfer characteristic.
- c) (5 marks) On another sketch of the static transfer characteristic, again with an inverter threshold of  $V_{DD}/2$ , show the operating region of each transistor over the range  $0 \leq V_{in} \leq V_{DD}$ .
- d) (5 marks) Where is the point of maximum power dissipation, and what is the value of power dissipation at this point? Assume the inverter output is unloaded.

#### Question 4 (Total 20 marks)

The layout of an integrated circuit block is shown below. External connections to the block are made through points A-E.

- a) (10 marks) Extract the transistor level schematic of this circuit.
- b) (5 marks) Determine the gate-level function of the circuit.
- c) (5 marks) Give two examples of masks not shown in the layout but which would be required for a modern CMOS process. Explain carefully what the masks are used for and why the steps are required.



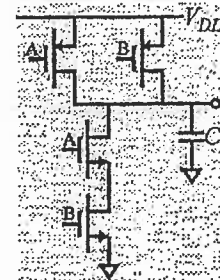
#### Question 5. (Total 20 marks)

Discuss in detail (approximately one page each) any four of the terms or topics given below. Your answer should concentrate on the context of an integrated circuit CAD environment. Each definition is worth 5 marks, and all are equally weighted.

- (a) Transistor compact model.
- (b) Standard cell pitch.
- (c) Behavioral simulation.
- (d) Layout extraction.
- (e) Harmonic balance simulation.
- (f) Field-programmable gate array.

### Question 6. (Total 20 marks)

The schematic of a two-input NAND gate driving a capacitive load is shown to the right.



- a) (5 marks) Explain how  $R_{on}$  can be approximated for each device, and how this quantity can be used to estimate transient switching behavior.
- b) (5 marks) What is the worst case rise time condition for this gate?
- c) (5 marks) What is the worst case fall time condition for this gate?
- d) (5 marks) Considering your answers to parts (b) and (c), explain how the devices would be sized to ensure symmetrical rise and fall times.

### Question 7. (Total 20 marks)

- a) (4 marks) Define the term “sequential digital circuit”, and give an example.
- b) (16 marks) Show how  $C^2$ MOS and NORA-CMOS techniques can be used to improve the performance of sequential digital circuits.