

National Exams May 2011

98-Comp-A3, Computer Architecture

Duration: 3 hours

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to include in the answer paper a clear statement of what the ambiguity is and of any assumptions made.
2. This is a CLOSED BOOK EXAM.
No calculators are permitted.
3. FIVE (5) questions constitute a complete exam paper. The first five questions as they appear in the answer book will be marked.
4. All questions are of equal value.
5. Some questions require an answer in essay format. Clarity and organization of the answer are important.

Marking Scheme

1. (a) 10 marks, (b) 10 marks
2. case a: 5 marks, case b: 5 marks, case c: 10 marks
3. 20 marks
4. (a) 10 marks, (b) 10 marks
5. (a) 10 marks, (b) 10 marks
6. (a) 8 marks, (b) 6 marks, (c) 6 marks
7. (a) 10 marks, (b) 10 marks

1. There are two styles of processor architecture: RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer).
 - a) Explain briefly the main differences between these two styles of processor architecture.
 - b) The immediate addressing mode of a 32-bit processor uses only 16-bit operands. The instruction

`Load_Immediate Ri, #0xA020`

loads the hexadecimal value A020, sign extended, into processor register R_i . How can you load the value 0xFF84A020 into register R5 of that processor? Suggest a suitable instruction that would simplify this task and write a short sequence of instructions using it. Make sure to add comments to explain what each instruction does.

2. When a subroutine is called, the processor saves the return address to enable the calling program to continue execution after return from the subroutine. Consider the following possibilities for saving the return address:
 - a) In a processor register,
 - b) On a stack.

For each of these cases, explain what you need to do, anything, to make it possible for one subroutine to call another subroutine (subroutine nesting).

With each of these approaches, is it possible for a subroutine to call itself (subroutine recursion)? Explain why.

3. An interface circuit connects a character display device to the bus a computer. When the processor writes a byte of data into this interface, it is loaded into an 8-bit register. The timing of data transfers on the bus is controlled by a clock signal. To write a byte of data, the processor sends the address and data on the rising edge of the clock and sets a Write signal to 1. Data are loaded into the interface register on the following rising edge of the clock. At the same time, the interface sends a pulse with a width of one clock cycle on a line called New-data, to load the data byte into the display device. Design a circuit for this output interface. Explain briefly how the circuit operates.
4. A cache memory reduces the average memory access time seen by the processor.
 - a) Give a simple example to explain the statement above.
 - b) Many computers use more than one level of cache, often referred to as L1, L2, etc. The purpose of using an L2 cache is to reduce the miss penalty of the L1 cache, and in turn to reduce further the average memory access time seen by the processor. Would increasing the size of the L1 cache accomplish the same objective? If so, what limits the utility of this approach?

5. The condition code flags C and V indicate whether an arithmetic operation has resulted in a carry or overflow.
- Give an appropriate truth table to show that the logic expression $c_n \oplus c_{n-1}$ is a correct indicator of overflow in the addition of 2's-complement integers, where c_n is the carry-out from the sign-bit position and c_{n-1} is the carry-in to the sign-bit position.
 - In some processors, no condition code flags are provided. Instead, the desired condition can be detected using software instructions to examine the result of an operation. When adding two unsigned numbers, a carry results if the sum is smaller than either of the two numbers. Assume that a processor has the following instruction for unsigned numbers:

Compare-less-than-U R_i, R_j, R_k

It sets register R_i to 1 if the value in register R_j is less than that in register R_k .

The low and high-order halves of a double-precision number are stored in R_5 and R_6 , respectively. It is desired to add this number to another double-precision number in registers R_7 and R_8 and leave the sum in registers R_7 and R_8 . Give a sequence of instructions to perform this task. Ignore overflow.

6. In a computer with a virtual-memory system, the execution of an instruction may be interrupted when a page fault occurs.
- Give an example of a situation in which this could happen.
 - What information needs to be saved to enable the processor to complete execution of the interrupted instruction at a later time?
 - An alternative is to abandon the interrupted instruction and completely re-execute it later. What needs to be done in this case?
7. Consider a long sequence of accesses to a disk with 8 ms average seek time, 3 ms average rotational delay, and a data transfer rate of 60 Mbytes/sec. The average size of a block being accessed is 64 Kbytes. Assume that each data block is stored in contiguous sectors.
- Assuming that the blocks are randomly located on the disk, estimate the average percentage of the total time occupied by seek operations and rotational delays.
 - Suppose that 20 blocks are transferred in sequence from adjacent cylinders, reducing seek time to 1 ms. The blocks are randomly located on these cylinders. What is the total transfer time?