

**National Exams
May 2011**

Phys-A5: Semiconductor Devices & Circuits

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate must submit with the answer paper, a clear statement of any assumption made.
2. Candidates may use one of two calculators, the Casio or Sharp approved models.
3. This is a CLOSED BOOK EXAM.
Useful constants and equations have been annexed to the exam paper.
4. Any FIVE (5) of the SEVEN (7) questions constitute a complete exam paper.
The first five questions as they appear in the answer book will be marked.
5. When answering questions, candidates must clearly indicate units for all parameters used or computed.

Marking scheme

<i>Questions</i>	<i>Marks</i>					
1	(a) 7	(b) 4	(c) 4	(d) 5		
2	(a) 10	(b) 4	(c) 6			
3	(a) 3	(b) 4	(c) 5	(d) 4	(e) 4	
4	(a) 2	(b) 2	(c) 4	(d) 4	(e) 4	(f) 4
5	(a) 2	(b) 3	(c) 3	(d) 8	(e) 4	
6	(a) 5	(b) 5	(c) 5	(d) 5		
7	(a) 8	(b) 6	(c) 3	(d) 3		

1. An unknown semiconductor operating at a temperature of $T = 300 \text{ }^\circ\text{K}$ has a band gap $E_g = 1.1 \text{ eV}$ with $N_c = N_v$. It is doped with a donor concentration of $N_d = 10^{15} / \text{cm}^3$ to set the donors energy level E_D at 0.2 eV below the conduction band energy level E_C . The Fermi level E_F is 0.25 eV below the conduction band energy level E_C . These conditions are illustrated in Figure 1.

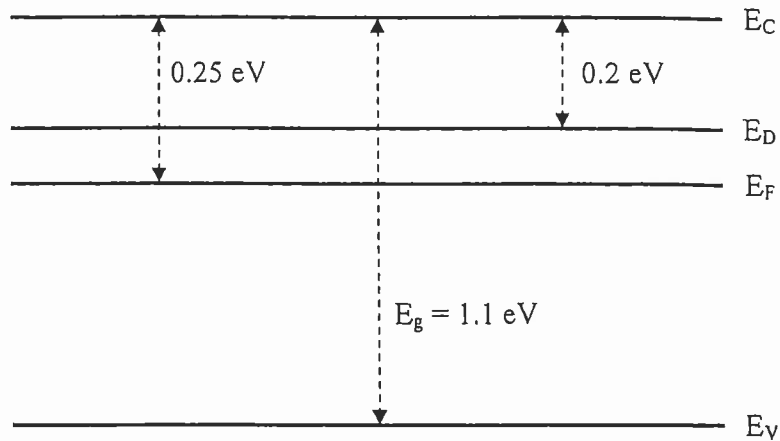


Figure 1 Energy band diagram for unknown semiconductor

- 7 pts (a) Using the Fermi-Dirac distribution function, show that the concentration of electrons n_o in this semiconductor at $T = 300 \text{ }^\circ\text{K}$ is equal to $8.73 \times 10^{14} / \text{cm}^3$.
- 4 pts (b) Calculate the values of N_c and N_v of this semiconductor at $T = 300 \text{ }^\circ\text{K}$.
- 4 pts (c) Show that the concentration of holes p_o in this semiconductor at $T = 300 \text{ }^\circ\text{K}$ is equal to $8.3 \times 10^{14} / \text{cm}^3$.
- 5 pts (d) What is the concentration of intrinsic carriers n_i in this semiconductor at $T = 300 \text{ }^\circ\text{K}$?

2. An abrupt silicon $p-n$ junction of constant cross section $A = 10^{-4} \text{ cm}^2$ has the following properties at a temperature of $T = 300 \text{ }^\circ\text{K}$:

p side

$$N_a = 10^{17} \text{ cm}^{-3}$$

$$\tau_n = 0.1 \text{ } \mu\text{s}$$

$$\mu_p = 200 \text{ cm}^2/(\text{V}\cdot\text{s})$$

$$\mu_n = 700 \text{ cm}^2/(\text{V}\cdot\text{s})$$

n side

$$N_d = 10^{15} \text{ cm}^{-3}$$

$$\tau_p = 10 \text{ } \mu\text{s}$$

$$\mu_n = 1300 \text{ cm}^2/(\text{V}\cdot\text{s})$$

$$\mu_p = 450 \text{ cm}^2/(\text{V}\cdot\text{s})$$

This $p-n$ junction is used as a diode in the circuit shown in Figure 2 where the diode bias voltage V_d is obtained by using a 5 V DC voltage source and a variable resistor R .

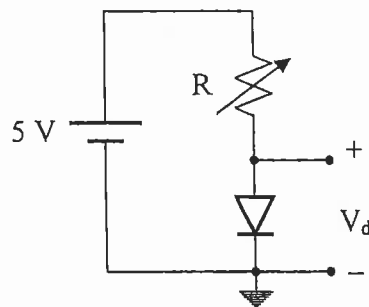


Figure 2

- 10 pts (a) If resistor R is adjusted such that the diode is forward biased with $V_d = +0.7$ volt, what is the value of the forward current in the diode?
- 4 pts (b) When resistor R is adjusted such that $V_d = +0.65$ volt, the value of the forward current in the diode is $315 \text{ } \mu\text{A}$. In these conditions, what is the value of resistor R ?
- 6 pts (c) If the polarity of the 5 V DC voltage source is reversed and resistor R is adjusted such that the diode is reversed biased with $V_d = -0.5$ volt, what is the value of the reverse current in the diode?

3. An engineer is asked to design a first order high pass filter described by the following equation:

$$F(s) = \frac{V_o}{V_i} = \frac{\pm 10^2 s}{s + 10^3}$$

where the sign of $F(s)$ is optional.

Looking in a filter cook book, the engineer finds that the two circuits shown in Figure 3 are both possible candidates to realize a first order high pass filter.

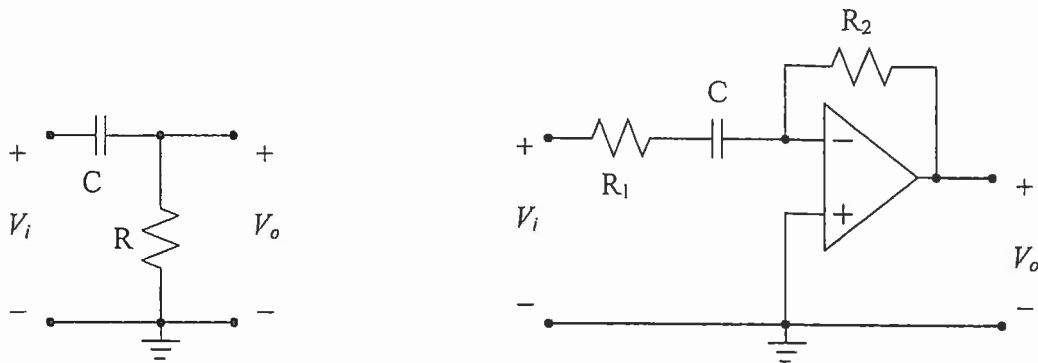


Figure 3

- 3 pts (a) Find the value (in dB) of the magnitude of $F(s)$ at very high frequencies.
- 4 pts (b) What is the required corner frequency ω_H of this filter? *(express your answer in rad/s)*
- 5 pts (c) Find the value (in dB) of the magnitude of $F(s)$ at a frequency of $\omega = 500$ rad/s.
- 4 pts (d) Briefly explain why the circuit on the left hand side of Figure 3 cannot be used to realize the required filter.
- 4 pts (e) The engineer knows that the circuit on the right hand side of Figure 3 must be used and decides to utilize a value of $50 \text{ K}\Omega$ for resistor R_2 .
What must be the values of resistor R_1 and capacitor C in order to obtain the required corner frequency ω_H of the filter? *(express your answer in μF)*

4. A single stage amplifier is shown in Figure 4. The active device in the circuit is biased such that its small signal parameters at the operating point are $g_m = 4 \text{ mA/V}$ and $r_o = 200 \text{ k}\Omega$.

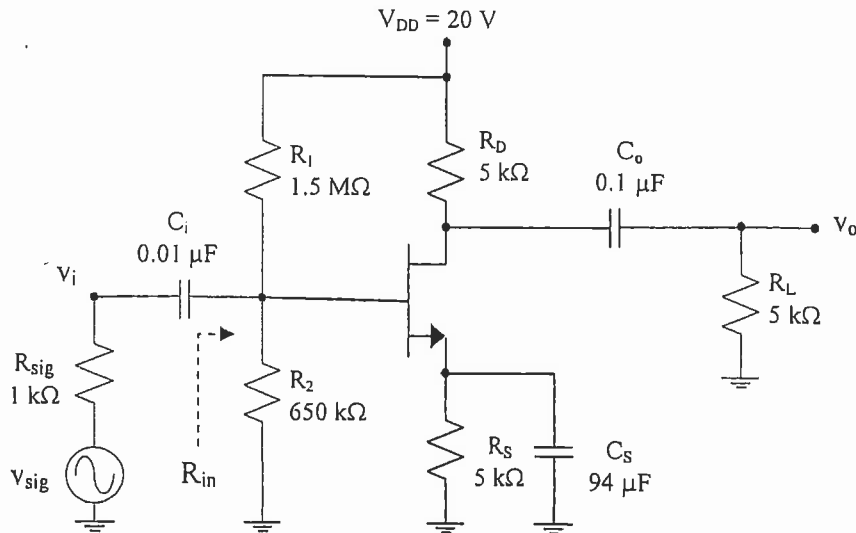


Figure 4

- 2 pts (a) What type of transistor is used in the circuit?
Select one out of the following six types:
- | | | |
|---------|----------------|------------------|
| NPN-BJT | N-channel JFET | N-channel MOSFET |
| PNP-BJT | P-channel JFET | P-channel MOSFET |
- 2 pts (b) What is the name of the configuration of this amplifier?
Select one out of the following six configurations:
- Bypassed common emitter
 - Unbypassed common emitter
 - Bypassed common drain
 - Unbypassed common drain
 - Bypassed common source
 - Unbypassed common source
- 4 pts (c) Draw the mid-band small signal equivalent circuit of the amplifier and clearly indicate the name and value of each component.
- 4 pts (d) What is the value of the input resistance R_{in} ?
- 4 pts (e) Calculate the mid-band voltage gain $A_m = v_o/v_{sig}$.
- 4 pts (f) If the values of the capacitors are such that the time constant involving C_o creates the dominant pole in the frequency response of the amplifier, what is the value of the lower corner frequency f_L of the amplifier? (express your answer in Hz)

5. Figure 5a shows a CMOS inverter and its voltage transfer characteristic. The width and length of each transistor are chosen such that $W_p/L_p = W_n/L_n = 2$. Figure 5b represents a complex CMOS logic gate.

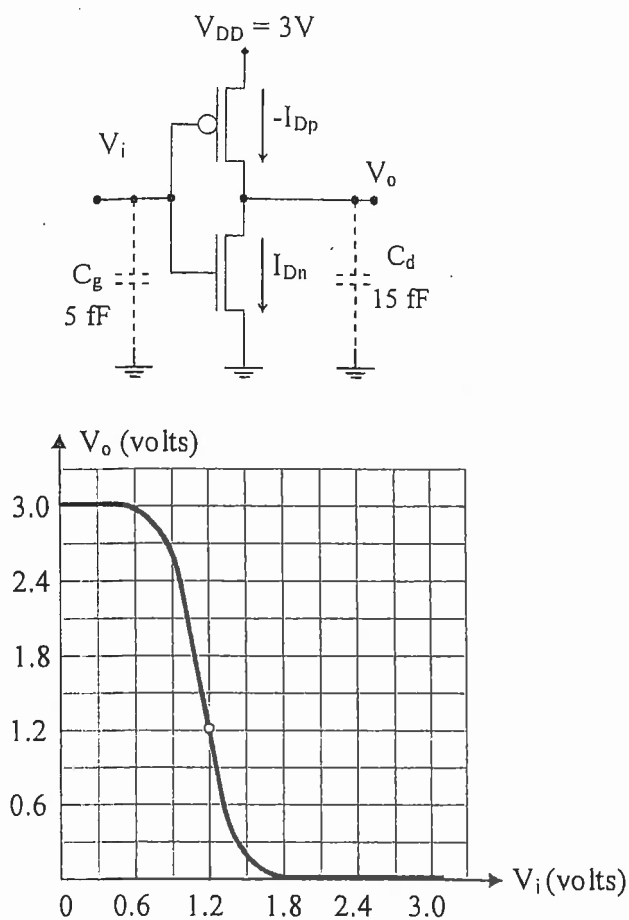


Figure 5a

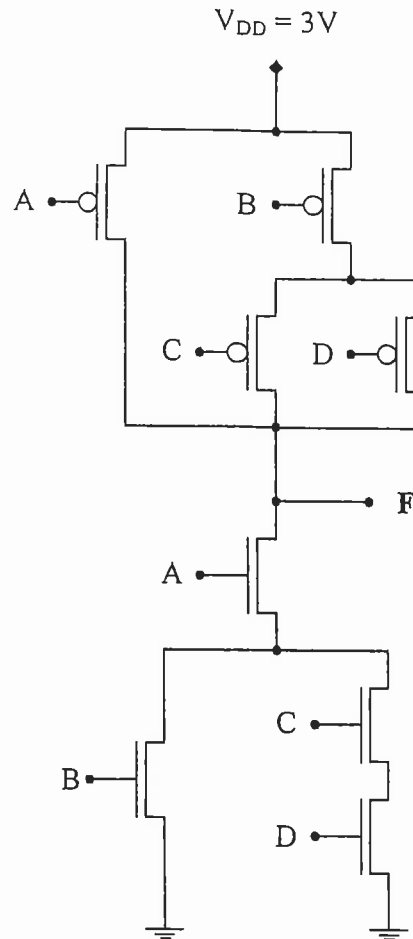


Figure 5b

- 2 pts (a) What are the values of V_{OH} and V_{OL} for the inverter?
- 3 pts (b) Briefly explain how to change the properties of the NMOS and/or the PMOS transistors in order for the curve to shift right and go through point $V_o = V_i = 1.5$ V to make it symmetrical.
- 3 pts (c) Briefly explain what limits the fan-out of CMOS logic gates.
- 8 pts (d) If $V_{tn} = -V_{tp} = 0.5$ V, what is the value of the ratio k_n/k_p of this inverter?
(Hint: the curve goes trough point $V_o = V_i = 1.2$ V)
- 4 pts (e) Find a Boolean expression for the output function F generated by the complex logic gate of Figure 5b in terms of input variables A,B,C,D.

6. Figure 6 shows the basic diagram of a 12-bit dual-slope analog-to-digital converter (ADC) and its typical time response for a full conversion. This ADC is based on a clock running at 1 MHz and it has a reference voltage $V_{ref} = +10$ V. The range of the analog input voltage V_n is 0 to -10 V. The fixed interval T_1 for the first slope is taken as the time for the internal counter to accumulate a full 12-bit count.

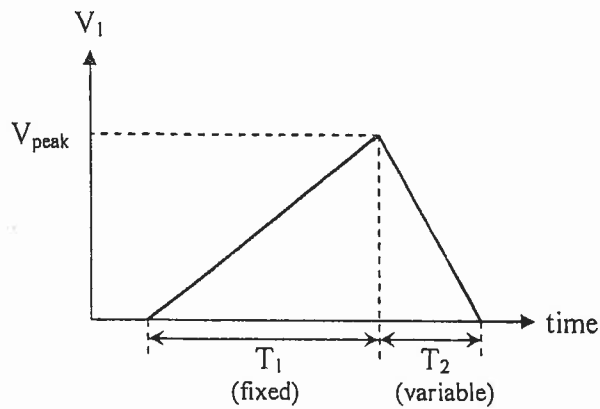
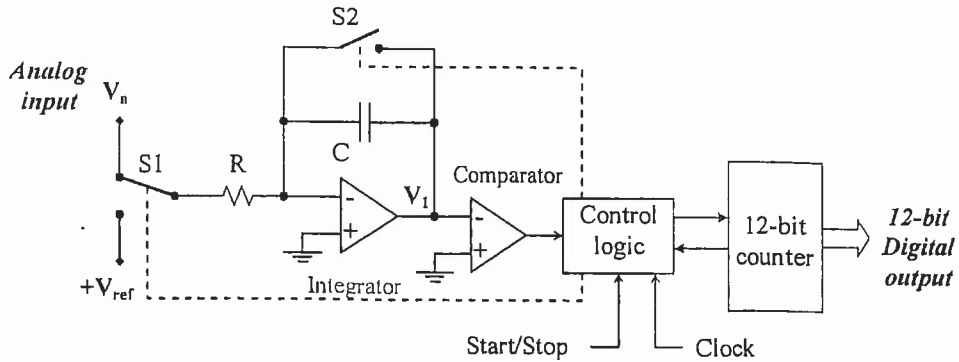


Figure 6

- 5 pts (a) What is the total time to convert an analog input voltage V_a equal to -5 V?
(express your answer in ms)
- 5 pts (b) When the input voltage $V_a = -10$ V, the peak voltage reached at the output of the integrator is $V_{peak} = +10$ V. What is the time constant $\tau = RC$ of the integrator?
- 5 pts (c) If, through aging, R increases by 2% and C decreases by 1%, what does V_{peak} become when the input voltage $V_a = -10$ V?
- 5 pts (d) Explain why the conversion accuracy of this ADC is not affected by the aging of the R and C components of the integrator circuit.

7. An engineer is tasked to design a precision half-wave rectifier to be used for a high accuracy instrumentation system. The engineer decides to use the *superdiode* circuit shown in Figure 7a to practically eliminate the diode offset voltage V_{off} which is present in the simple half-wave rectifier using a single diode as illustrated in Figure 7b.

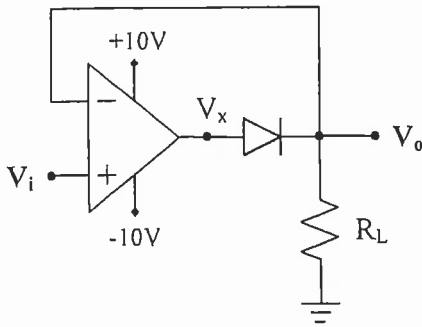


Figure 7a

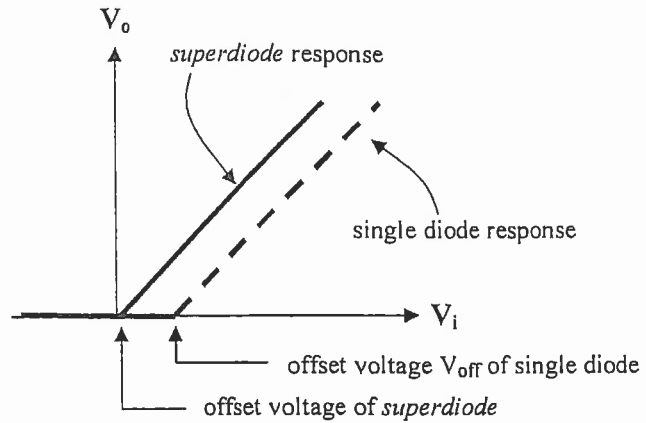


Figure 7b

- 8 pts (a) If the open loop gain of the operational amplifier is $A = 105,000$ and if the diode offset voltage is $V_{off} = 0.48$ V, show that the *superdiode* offset voltage V_{off} is less than $5 \mu\text{V}$.
- 6 pts (b) Other than reducing the diode offset voltage, what other advantage does the *superdiode* circuit have over the single diode circuit?
- 3 pts (c) What must be the reverse bias voltage rating of the diode?
- 3 pts (d) If the input signal is a sinusoid of the form $V_i(t) = 5 \sin \omega t$ and if the minimum value of the load resistor R_L is 250 ohms, what must be the output current rating of the operational amplifier?

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USEFUL CONSTANTS AND EQUATIONS

- (1) $1 \text{ \AA} = 10^{-10} \text{ m} = 10^{-8} \text{ cm} = 10^{-4} \text{ \mu m}$
 (2) $q = 1.6 \times 10^{-19} \text{ C}$
 (3) $k = 1.38 \times 10^{-23} \text{ J/}^\circ\text{K} = 8.62 \times 10^{-5} \text{ eV/}^\circ\text{K}$ [At $T = 300^\circ\text{K}$, $kT/q \approx 26 \text{ mV}$ $kT = 0.026 \text{ eV}$]

- (4) For silicon (Si) at $T = 300^\circ\text{K}$: $n_i = 1.5 \times 10^{10} / \text{cm}^3$
 (5) $\epsilon_{\text{Si}} = 1.04 \times 10^{-12} \text{ F/cm}$
 (6) $\epsilon_{\text{SiO}_2} = 0.345 \times 10^{-12} \text{ F/cm}$ [farad: $1 \text{ F} = 1 \text{ C/V}$] [siemens: $1 \text{ mS} = 1 \text{ mA/V} = 1 \text{ mmho}$]

- (7) $f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$
 (8) $n_o + N_a = p_o + N_d$
 (9) $n_o p_o = n_i^2$
 (10) $n_o = N_c e^{(E_F - E_c)/kT} = n_i e^{(E_F - E_i)/kT}$
 (11) $p_o = N_v e^{(E_v - E_F)/kT} + n_i e^{(E_i - E_F)/kT}$
 (12) $n_i = \sqrt{N_c N_v} e^{-E_g/2kT}$
 (13) $V_o = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$
 (14) $W = \sqrt{\frac{2\epsilon_{\text{Si}} V_o}{q} \left(\frac{1}{N_a} + \frac{1}{N_d} \right)}$
 (15) $x_{po} = \frac{W N_d}{N_a + N_d}$ $x_{no} = \frac{W N_a}{N_a + N_d}$

- (16) $\sigma = q(n_o \mu_n + p_o \mu_p)$
 (17) $\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q}$ $L_n = \sqrt{D_n \tau_n}$ $L_p = \sqrt{D_p \tau_p}$
 (18) $n_n p_n = n_i^2 = n_p p_p$
 (19) $I = I_o (e^{\frac{qV}{kT}} - 1) = qA \left(\frac{D_p}{L_p} p_n + \frac{D_n}{L_n} n_p \right) (e^{\frac{qV}{kT}} - 1)$
 (20) $J = \frac{I}{A} = \sigma \mathcal{E}$
 (21) $R = \frac{L}{\sigma A}$

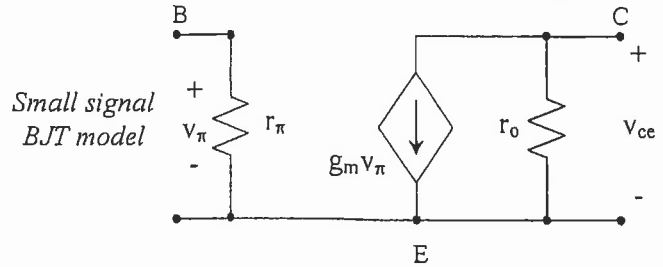
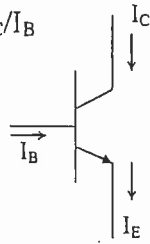
BJT relationships and model

(22) $I_C = \beta I_B$ where $\beta = I_C/I_B$

(23) $I_E = I_B + I_C$

(24) $g_m = I_C/V_T$

(25) $r_\pi = V_T/I_B$



MOS relationships and model

(26) $C_i = \frac{\epsilon_{SiO_2}}{d}$

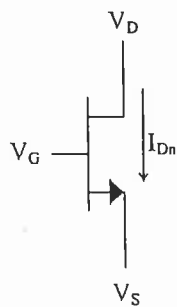
(27) $V_T = \Phi_{ms} + 2\phi_F - \frac{1}{C_i}(Q_i + Q_d)$

(28) $I_{Dn} = (k_n/2)(V_{GSn} - V_{tn})^2$ when $V_{DSn} > V_{GSn} - V_{tn}$

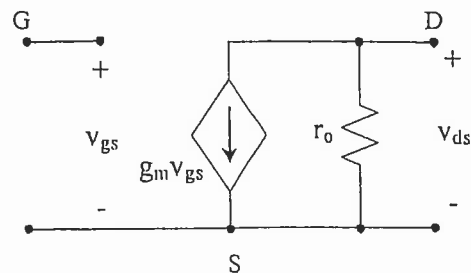
(29) $I_{Dn} = (k_n/2)[2(V_{GSn} - V_{tn})(V_{DSn}) - (V_{DSn})^2]$ when $V_{DSn} < V_{GSn} - V_{tn}$

(30) $I_{Dp} = -(k_p/2)(V_{GSp} - V_{tp})^2$ when $V_{DSp} < V_{GSp} - V_{tp}$

(31) $I_{Dp} = -(k_p/2)[2(V_{GSp} - V_{tp})(V_{DSp}) - (V_{DSp})^2]$ when $V_{DSp} > V_{GSp} - V_{tp}$



Small signal FET model



Integrator circuit relationships

(32) $V_o(t) = -\frac{1}{RC} \int_0^t V_i(t) dt$ $\frac{V_o(s)}{V_i(s)} = \frac{-1}{sRC}$