National Exams December 2012

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of a question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes into the examination room:

3. This paper contains **FIVE (5)** questions and comprises **eight (8)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in the answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and the marks for each part of questions are indicated in brackets.

7. Data on some relevant Digital ICs are provided in the Appendix. A PAL16L8 Data sheet is provided on page 6 (in the Appendix). It can be used to provide the solution of Problem 1, part (b-ii) and should be attached to your answer sheet.

1. (a) (i) Determine the Boolean expression for output Y of the circuit given in Figure Q1. Simplify the expression using Boolean algebra.

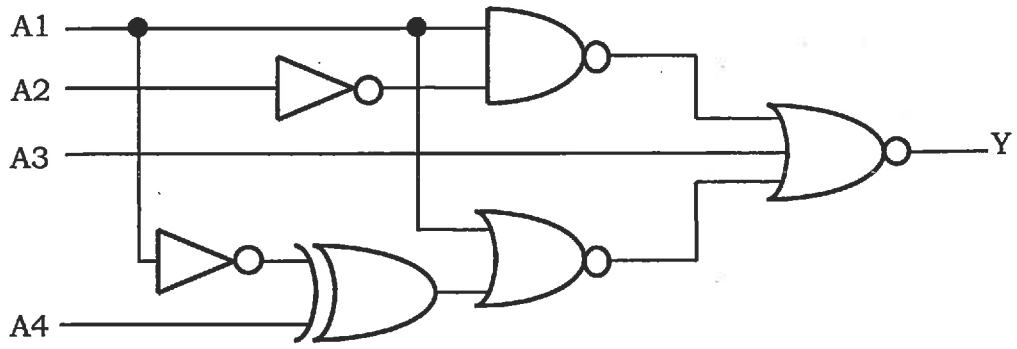


Figure Q1

(ii) Implement the circuit of Figure Q1 by using 2-input NOR gates only.

(5+5 marks)

(b) Three sensors, T, C and S measure the temperature, coolant and speed parameters of the engine of a military vehicle respectively. Followings are the conditions at which the outputs of sensors are at logic HIGH:

- Temperature > 195°F (T sensor output = 1)
- Coolant > 600ml (C sensor output = 1)
- Speed > 6000rpm (S sensor output = 1)

(i) Develop a Boolean expression for activating an engine warning buzzer when the temperature is greater than 195°F and either the coolant is less than or equal 600ml, or the speed is greater than 6000 rpm. Assume that a logic HIGH signal can activate the buzzer.

(ii) Implement the Boolean expression of part (b-i) using a PAL16L8 programmable logic device.

(7+8 marks)

2. A digital system is used to control the opening of entrance gates (G1 and G2) of a two-part (P1 and P2) parking garage. The entrance gate G1 leads to P1 part of the garage that has 114 parking spaces. G2 gate is used for vehicles to be parked in P2 that has 64 parking spaces. Both P1 and P2 parts of the garage have their own exit gates.

The P1 part of the garage is mainly used for parking where P2 part of the garage is only utilized when P1 is full. The parking in P2 is managed by the digital system by opening gate (G2) when P1 garage is full. Empty spaces in P1 are monitored by the system, and for an incoming vehicle, G2 gate is only opened when P1 is full. The main features of the digital system and its input and output signals are given below:

- One sensor each at entrance gates (G1 and G2) produces a positive TTL pulse when a vehicle enters P1 and P2 parts of the garage. A sensor each at the exit gates produces negative TTL pulse when a vehicle leaves the garage.
- The digital system monitors empty spaces in P1 and P2 garages by counting up when a vehicle enters and counts down when a vehicle leaves the garage through their respective gates.
- The system produces HIGH TTL level outputs to open the garage entrance gates where the exit gates are automatically opened when a vehicle arrives at these gates.

Design and implement the digital system using up/down counters (e.g. 74193) and other hardware (such as logic gates, flip-flops, etc.) to control the G1 and G2 entrance gates of the garage.

(25 marks)

3. A combination lock employs a synchronous sequential machine that has two inputs (X and Y) and an output (UnLock) as shown in Figure Q3. A logic HIGH output (UnLocK) is generated if and only if X remains LOW and the sequence of inputs received on Y at the preceding five clock ticks is 10101.

(a) Identify the type of sequential machine used in the combination lock and determine its number of states.

(4 marks)

Question No. 3 continues on Page 4

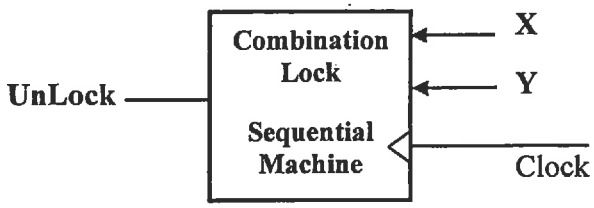


Figure Q3

(b) Draw the state diagram of the combination lock sequential machine.

(6 marks)

(c) Design and implement the sequential circuit by using D-type flip-flops.

(15 marks)

4. Design a logic circuit required to drive a 7-segment display when driven by a BCD input. Assume that the display requires an active-HIGH input to turn on an LED segment. The seven segments are shown in Figure Q4.

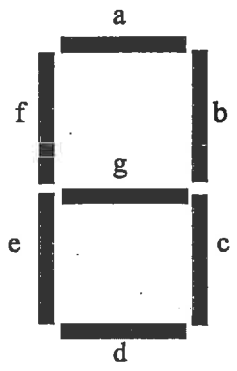


Figure Q4

(a) Construct the truth table and simplify all the output (logic) equations for 7 segments (a, b, c, d, e, f, and g) using the K-map method.

(10 marks)

Question No. 4 continues on Page 5

(b) Implement the logic circuit by using the minimum number of NAND gates and draw the logic diagram.

(15 marks)

5. Design a finite state machine with two inputs (**a** and **b**) and one output, **z**. The state table of the finite state machine is given below.

Present State	**Next State** ab= 00	01	10	11	**Output z**
S0	S0	S1	S1	S2	1
S1	S0	S2	S1	S0	0
S2	S1	S2	S0	S3	1
S3	S1	S2	S2	S3	1

(a) Draw the state diagram and determine the number of flip-flops required to implement the finite state sequential machine. Justify your answers.

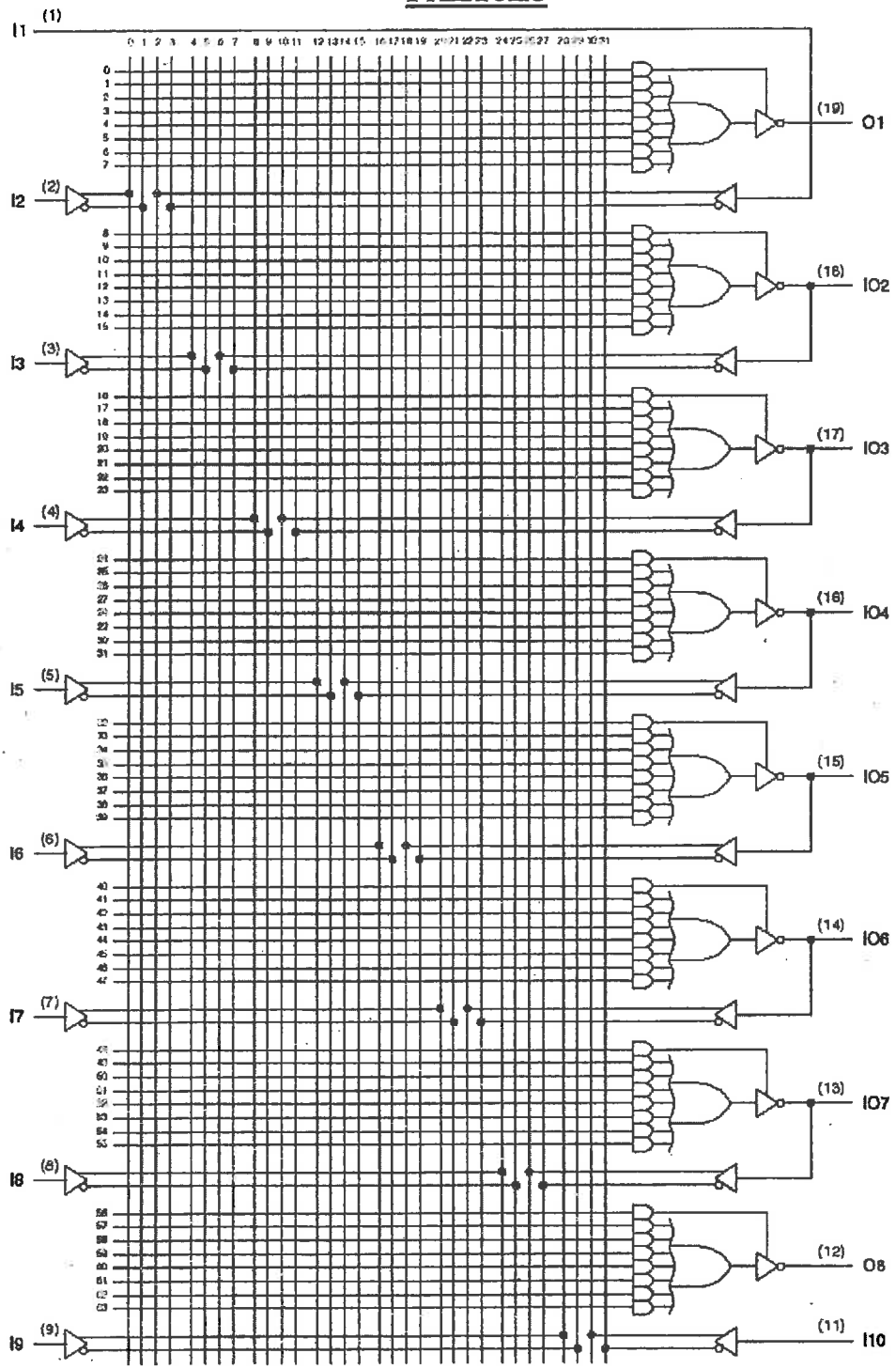
(8 marks)

(b) Use D-type flip-flops and other logic gates to design the above finite state machine. Show full details of your design.

(17 marks)

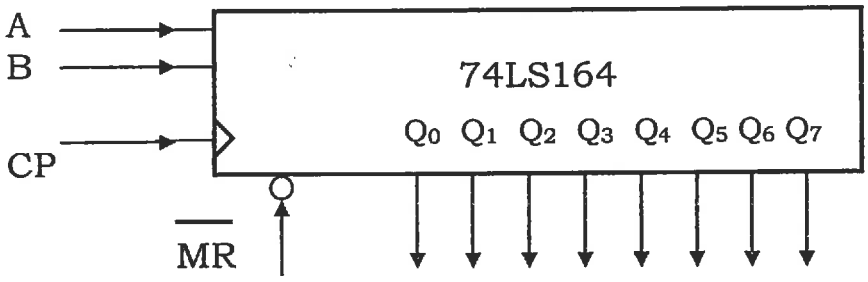
APPENDIX

PAL16L8



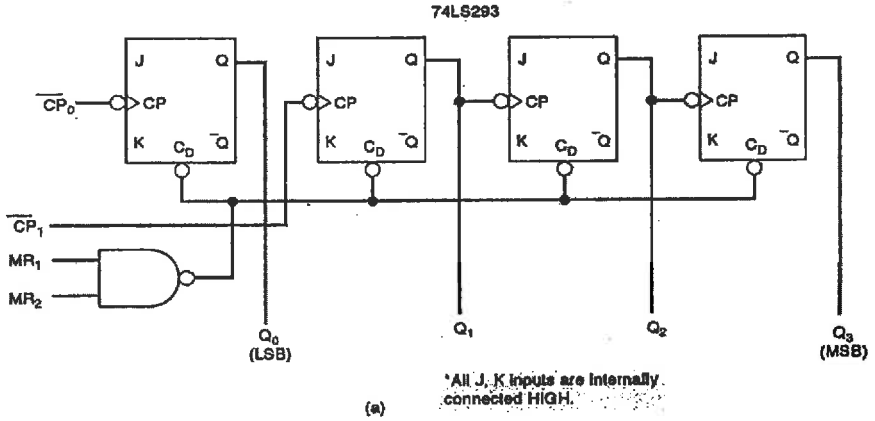
Counters and Other Data Sheets

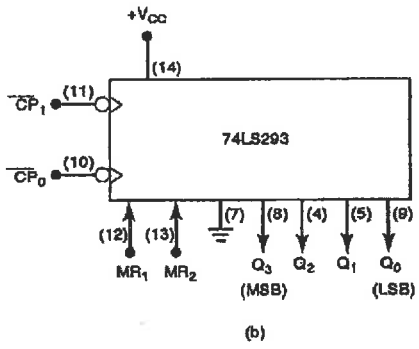
74LS164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0.
- Shift operation occurs at PGTs of the clock input CP.
- The $\overline{MR}$ input resets all FFs asynchronously on a LOW level.

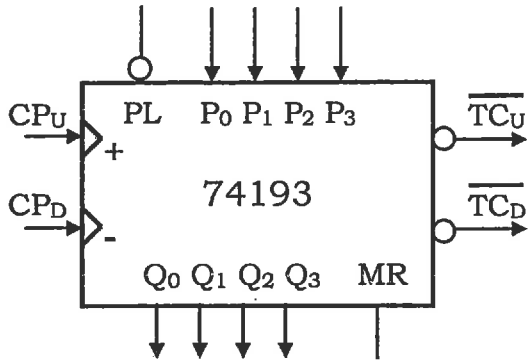
74LS293 : 3/4-bit counter





74193, 4-bit UP/ DOWN Counter

MR	$\overline{PL}$	CP_U	CP_D		Mode
H	x	x	x		Asynch Reset
L	L	x	x		Asynch Load
L	H	H	H		No change
L	H	↑	H		Count up
L	H	H	↑		Count down

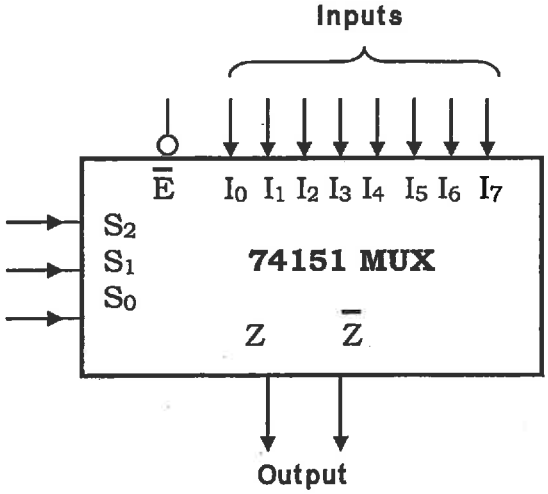


Pins	Description
CP_U	Count-up clock input
CP_D	Count-down clock input
MR	Asynchronous master reset input
$\overline{PL}$	Asynchronous parallel load input
P_0-P_3	Parallel data inputs
Q_0-Q_3	Flip-flop outputs
$\overline{TC_U}$	Terminal count-up (carry) output
$\overline{TC_D}$	Terminal count-down (borrow) output

74151 8-to-1 Multiplexer

Inputs Outputs

$\overline{E}$	S_2	S_1	S_0		Z	$\overline{Z}$
H	x	x	x		H	L
L	L	L	L		$\overline{I_0}$	I_0
L	L	L	H		$\overline{I_1}$	I_1
L	L	H	L		$\overline{I_2}$	I_2
L	L	H	H		$\overline{I_3}$	I_3
L	H	L	L		$\overline{I_4}$	I_4
L	H	L	H		$\overline{I_5}$	I_5
L	H	H	L		$\overline{I_6}$	I_6
L	H	H	H		$\overline{I_7}$	I_7



End of Paper