National Exams December 2012

07-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 2, (b) 2, (c) 2, (d) 2, (e) 2, (f) 2, total = 12
2. (a) 6, (b) 3, (c) 3, total = 12
3. (a) 3, (b) 6, (c) 3, total = 12
4. (a) 4, (b) 8, total = 12
5. (a) 4, (b) 8, total = 12
6. (a) 3, (b) 3, (c) 3, (d) 3, total = 12

The number beside each part above indicates the points that part is worth

1.- Given the following function in sum-of-products form:

$$f(A,B,C) = \overline{A}\cdot B\cdot \overline{C} + \overline{A}\cdot \overline{B} + \overline{B}\cdot C + A\cdot \overline{B}\cdot \overline{C}$$

(a) Prepare its truth table.

(b) Express f in canonical product-of-sums form.

(c) Express f in minimized product-of-sums form.

(d) Express f in minimized sum-of-products form.

For the next two parts (e) & (f) assume literal complements are available.

(e) Synthesize a NOR-only circuit for f using a minimum number of gates.

(f) Synthesize a NAND-only circuit for f using a minimum number of gates.

2.- A 3-bit counter advances through the sequence 001, 011, 010, 100, 111 back to 001 and repeats.

(a) Using the standard design process for synchronous counters, show how to implement this counter using D flip-flops. Include:

- state transition diagram,
- state transition table including flip-flop inputs, and
- a drawing of the final circuit implementing the counter.

(b) Check whether the counter is self-starting or not.

(c) Sketch the timing diagram for the counter showing its dynamic behavior, include:

- The clock waveform CLK, containing at least six clock pulses after $t = 0$, and
- The output waveforms Q_A, Q_B & Q_C, where Q_A is the output of flip-flop A (MSB[1]), Q_B is the output of flip-flop B and Q_C is the output of flip-flop C (LSB[1]).

Assume the $\overline{\text{CLR}}$ input of all flip-flops is temporarily held LOW during the clock cycles preceding time $t = 0$, then it goes HIGH.

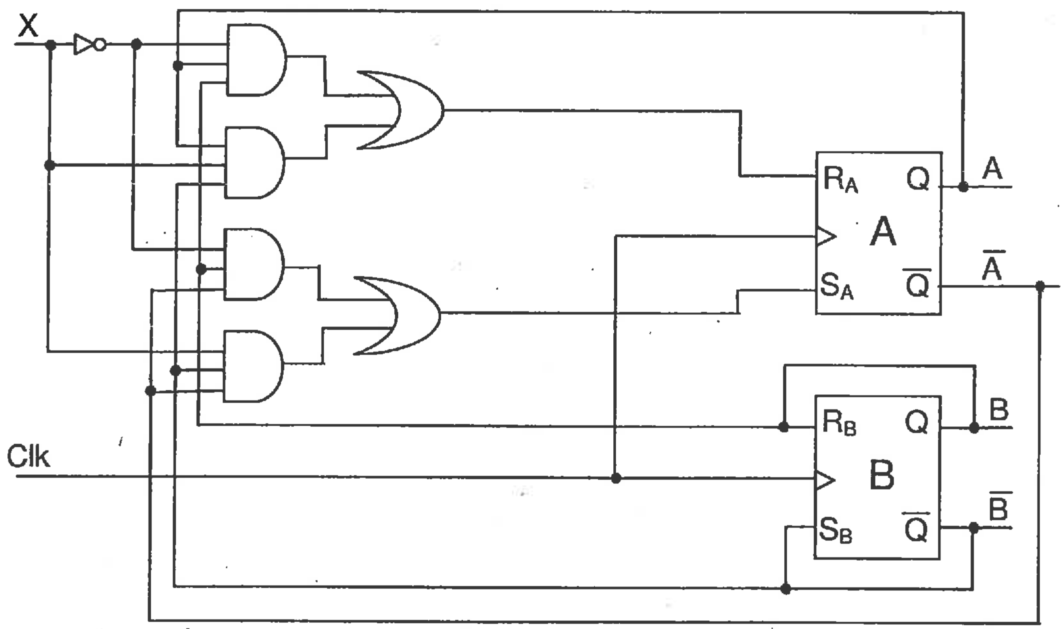
[1] MSB: most significant bit, LSB: least significant bit

3.- The following circuit contains two RS flip-flops.

(a) Write the logic expressions for R_A, S_A, R_B and S_B.

(b) Obtain the state transition table for the circuit.

(c) Sketch the state transition diagram for the circuit.



4.- Figure 1.1 below shows a circuit used to display six BCD digits in six common-cathode seven-segment displays. The LED arrangement for each seven-segment display is shown in parts 1.2 and 1.3 of the figure. A buffer chip is used to provide the current required to light up the LEDs as determined by Port B pin values, *i.e.* it provides all six displays with a logic '0' or a logic '1' as dictated by PB_7-PB_0, while adding the required driving capacity.

(a) Using a CPU accumulator register A with 'ldaa' (load accumulator A) and 'staa' (store accumulator A) instructions available, write a sequence of assembly instructions to display the number '4' on the seven-segment display #5.

Port B and Port D are memory mapped with addresses $1004 and $1008, respectively.

(b) Describe a way through which we can observe not just one digit lit as in part (a) above but all digits simultaneously showing '24.07.06' on the display arrangement shown in Figure 1.1. Include the sequence of steps to accomplish this as well as the bit patterns needed for Port B.

No need to include assembly instructions in part (b) just the algorithmic sequence.

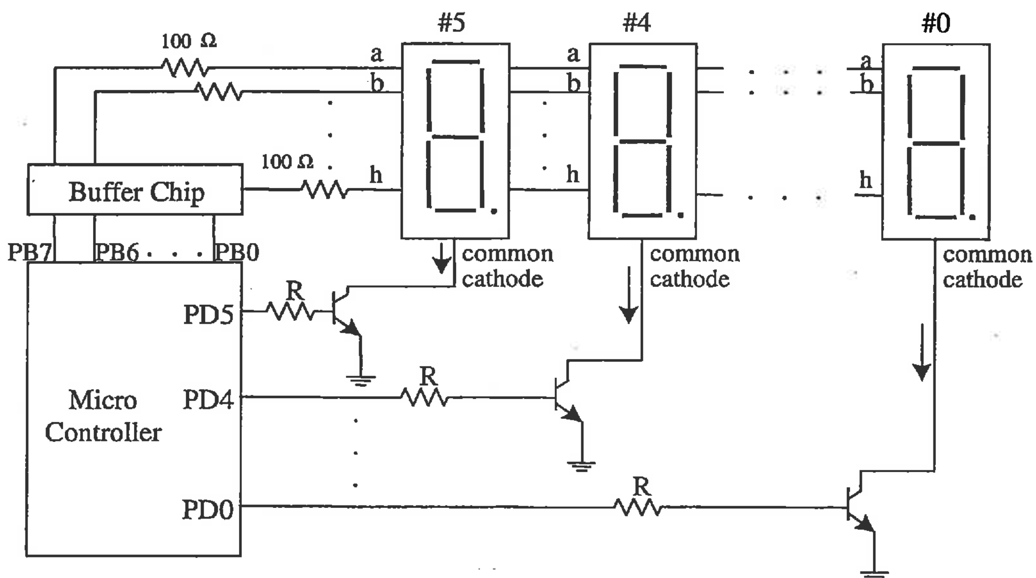


Fig 1.1. Port B and Port D together drive six seven-segment displays

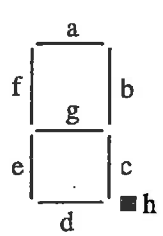


Fig 1.2. Seven-segment display

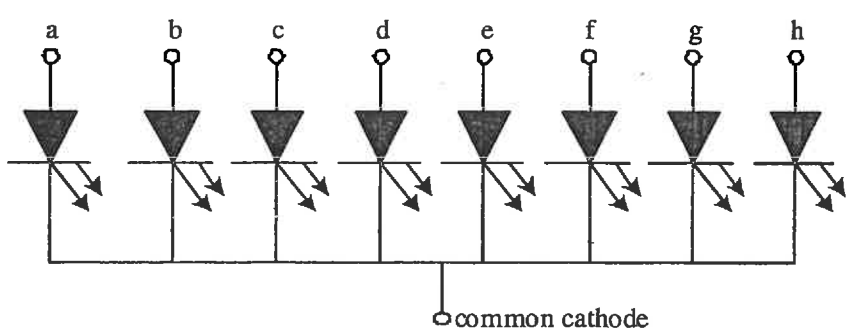
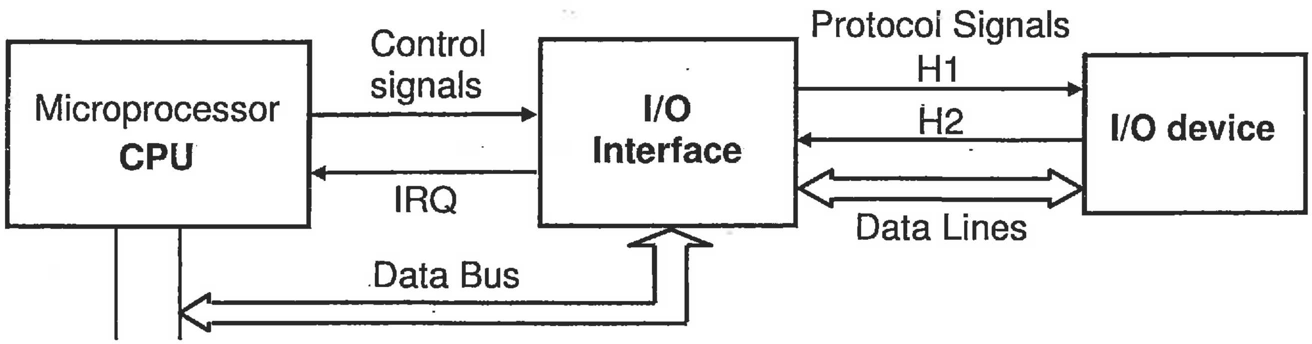


Fig 1.3. Common-cathode seven-segment display

5.- The diagram below shows the main elements participating in the parallel I/O of data.



(a) Mention the names of two commonly used methods for the CPU to communicate with the I/O interface.

(b) i. Mention three different parallel protocols used for implementing the data exchange between the I/O interface and the external I/O device.

ii. Mention the common names for protocol signals H1 and H2 associated with each protocol and describe how they are used in the input protocols and in the output protocols separately.

6.- Using the following memory chips, how many RAM chips will be needed to build a 512KB, 16-bit memory system for a 16-bit microprocessor? Justify your answer for each case. The memory is to be designed so that 16-bit data can be accessed in one read/write operation.

(a) 256K x 1 RAM

(b) 256K x 4 RAM

(c) 256K x 8 RAM

(d) 64K x 8 RAM

Note: KB = KiloByte, $1K = 2^{10}$

Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot\overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification