National Exams May 2012

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring the following into the examination room:
   (i) One hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **SIX (6)** questions and comprises **seven (7)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and the marks for each question part are indicated in brackets.

7. Data on some relevant Digital ICs are provided in the Appendix.

1. A combinational logic circuit is needed to divide a 3-bit binary number ($A_2A_1A_0$) by a constant 3_{10}. The output of the circuit (X) is the quotient as shown in Figure Q1.

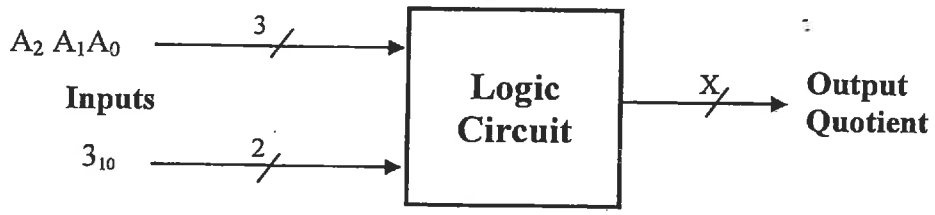


Figure Q1

(a) Determine the number of input and output variables.

(4 marks)

(b) Construct the truth table of the circuit indicating the input and output variables.

(7 marks)

(c) Simplify each output function and write the reduced Boolean functions of each output.

(7 marks)

(d) Implement the combinational logic circuit developed in part (c) by using minimum number of logic gates.

(7 marks)

2. (a) Describe the internal architecture of typical FPGA devices.

(6 marks)

(b) Design a 6-bit shift-right register using JK-type flip-flops and other logic gates if required.

(10 marks)

(c) Implement a 6-bit ring counter by using a suitable shift register. Briefly describe its operation.

(6+3 marks)

3. A digital circuit monitors a public hall that has 121 seating capacity. The circuit provides an indication of a full hall by illuminating a FULL display sign. The hall has three entrance/exit gates. The main features of the system are given below:

- A sensor at each entrance/exit gates produces an entry TTL pulse when a person enters the gate.
- A sensor at the entrance/exit gates also produces an exit TTL pulse when a person leaves the hall.
- The circuit counts down when a person enters and counts up when a person leaves the garage.
- The circuit produces a HIGH TTL output when the hall is full. This HIGH output signal is used to illuminate the FULL sign.
- The circuit output changes to LOW when an empty seat becomes available in the hall.

Design and implement the digital circuit by using suitable sequential devices and logic gates.

(25 marks)

4. (a) Briefly explain the working of tri-state buffers. Construct an 8-bit wide bi-directional tri-state buffer (data transceiver) by using eight single-bit tri-state buffers and any other gates (if needed). A block diagram of an 8-bit transceiver is shown in Figure Q4 with two control signals, DIR and ENABLE. DIR controls the direction of transfer (A-to-B or vice versa) while tri-state buffers are enabled with the ENABLE signal.

(16 marks)

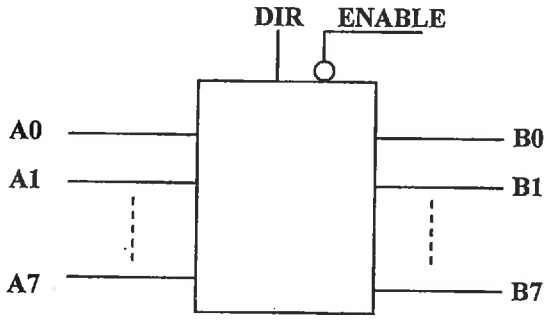


Figure Q4

(b) Identify the similarities of 2's complement and sign magnitude representation of binary numbers. Provide an example for each of both representations to support your answer.

(9 marks)

5. (a) List at least two useful applications of parity and explain how parity is used for these applications.

(7 marks)

(b) Design á combinational logic circuit with a minimum number of components that generate an even parity signal for an 8-bit data.

(10 marks)

(c) Study the JK flip-flop circuit of Figure Q5 as given below with three inputs A, B, and C. Determine the output Z at the clock transitions for all the combinations of the inputs.

(8 marks)

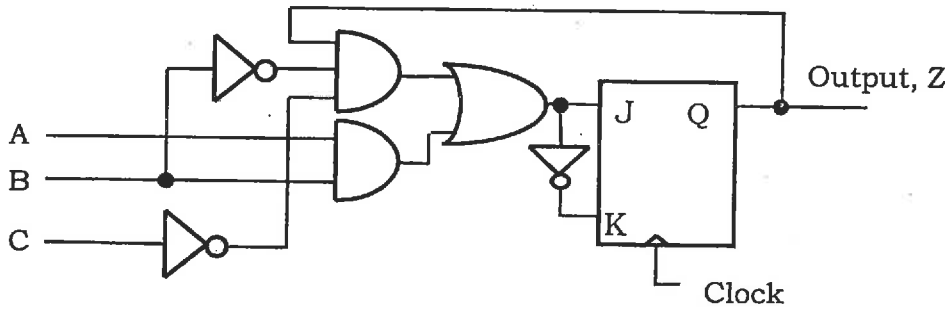


Figure Q5

6. Design a synchronous sequential circuit that checks a serial ASCII datum for odd parity. The circuit should have two inputs SYNC and DATA in addition to CLOCK and one (Moore type) output i.e. ERROR as shown in Figure Q6.

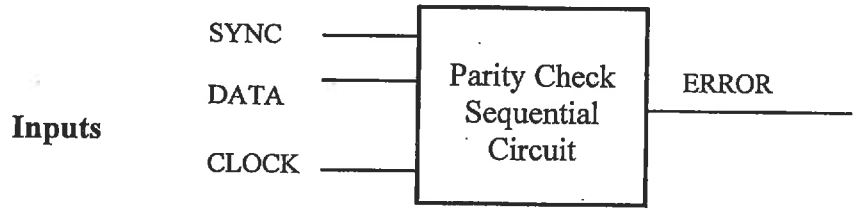


Figure Q6

(a) Develop a State Diagram and Table that does the job by using the minimum number of states.

(13 marks)

Question No. 6 continues on Page 5

(b) Design and implement the Parity Check circuit by using D-type flip-flops.

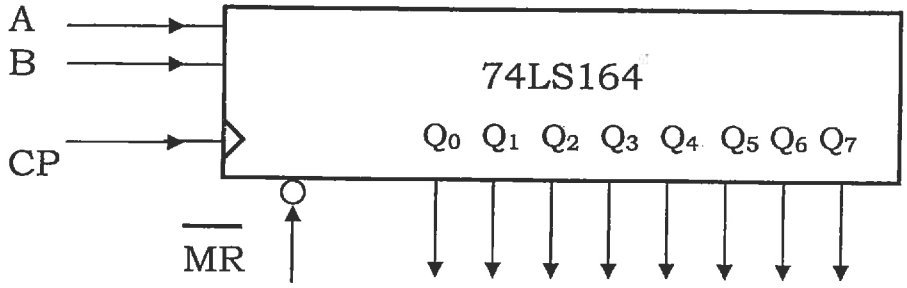
(12 marks)

End of Question 6

APPENDIX

Some Useful Data Sheets

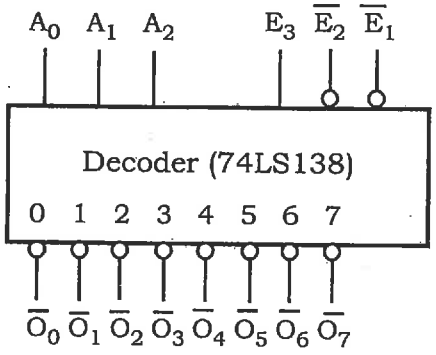
74LS164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0.
- Shift operation occurs at PGTs of the clock input CP.
- The $\overline{MR}$ input resets all FFs asynchronously on a LOW level.

Decoder Data Sheet

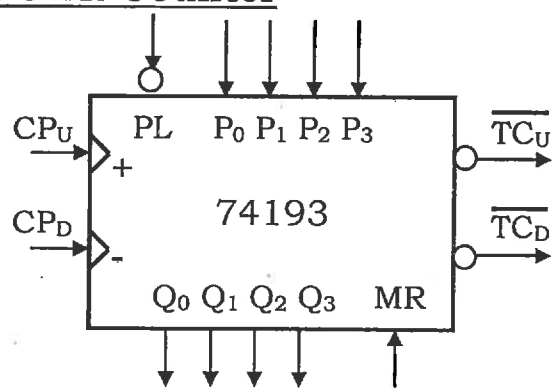
74LS138: 3-to-8 Decoder



Inputs			Outputs
$\overline{E}_1$	$\overline{E}_2$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled - all HIGH
x	1	x	Disabled - all HIGH
x	X	0	Disabled - all HIGH

74193, 4-bit UP/DOWN Counter

MR	$\overline{PL}$	CP_U	CP_D		Mode
H	x	x	x	:	Asynch reset
L	L	x	x		Asynch Load
L	H	H	H		No change
L	H	↑	H		Count up
L	H	H	↑		Count down



Pins	Description
CP_U	Count-up clock input
CP_D	Count-down clock input
MR	Asynchronous master reset input
$\overline{PL}$	Asynchronous parallel load input
P_0-P_3	Parallel data inputs
Q_0-Q_3	Flip-flop outputs
$\overline{TC_U}$	Terminal count-up (carry) output
$\overline{TC_D}$	Terminal count-down (borrow) output

END OF PAPER