

National Exams December 2015

**07-Elec-A4, Digital Systems & Computers**

3 hours duration

**NOTES:**

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.
2. This is a Closed Book exam.  
Candidates may use one of two calculators, the Casio or Sharp approved models.
3. FIVE (5) questions constitute a complete exam.  
You are required to answer questions 1, 2, 4 and 6.  
You have a choice of answering question 3 or question 5.
4. Questions 1, 2, 4 and 6 are worth 12 points.  
Questions 3 and 5 are worth 16 points.  
For a detailed breakdown see marking scheme on next page.

**Marking Scheme**

1. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
2. (a) 9, (b) 3, total = 12
3. (a) 2, (b) 3, (c) 5, (d) 3, (e) 3, total = 16
4. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
5. (a) 6, (b) 6, (c) 4, total = 16
6. (a) 3, (b) 3, (c) 3, (d) 3, total = 12

The number beside each part above indicates the points that part is worth

1.- Given the following function in sum of products form:

$$f(A, B, C) = A \cdot B \cdot \overline{C} + B \cdot C + A \cdot \overline{B} \cdot C$$

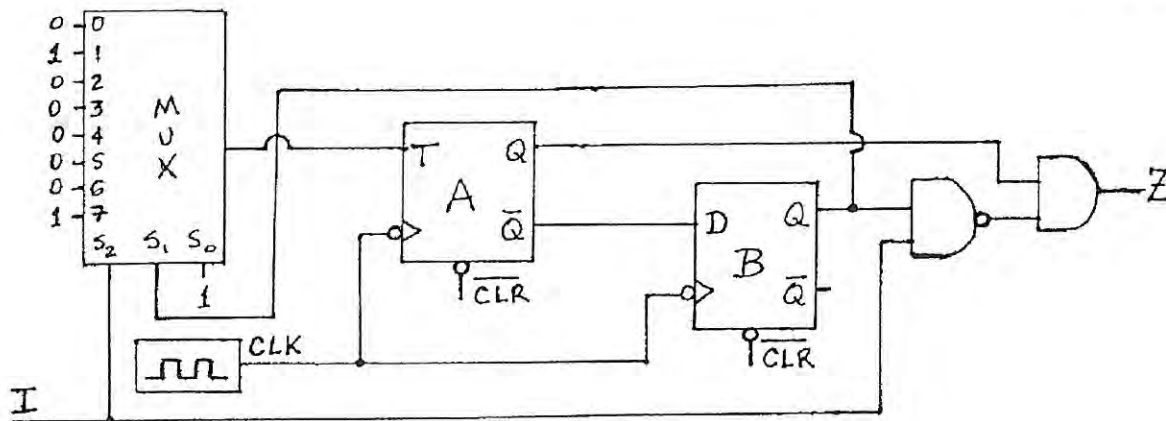
- (a) Prepare its truth table. [3 pts]
- (b) Express  $f$  in canonical product of sums form. [3 pts]
- (c) Use Karnaugh maps (K-maps) to express  $f$  in minimized product of sums form. [3 pts]
- (d) Synthesize a NOR-only circuit for  $f$  with a minimum number of gates. [3 pts]

2.- A circuit is needed to start and stop counting clock pulses on command.

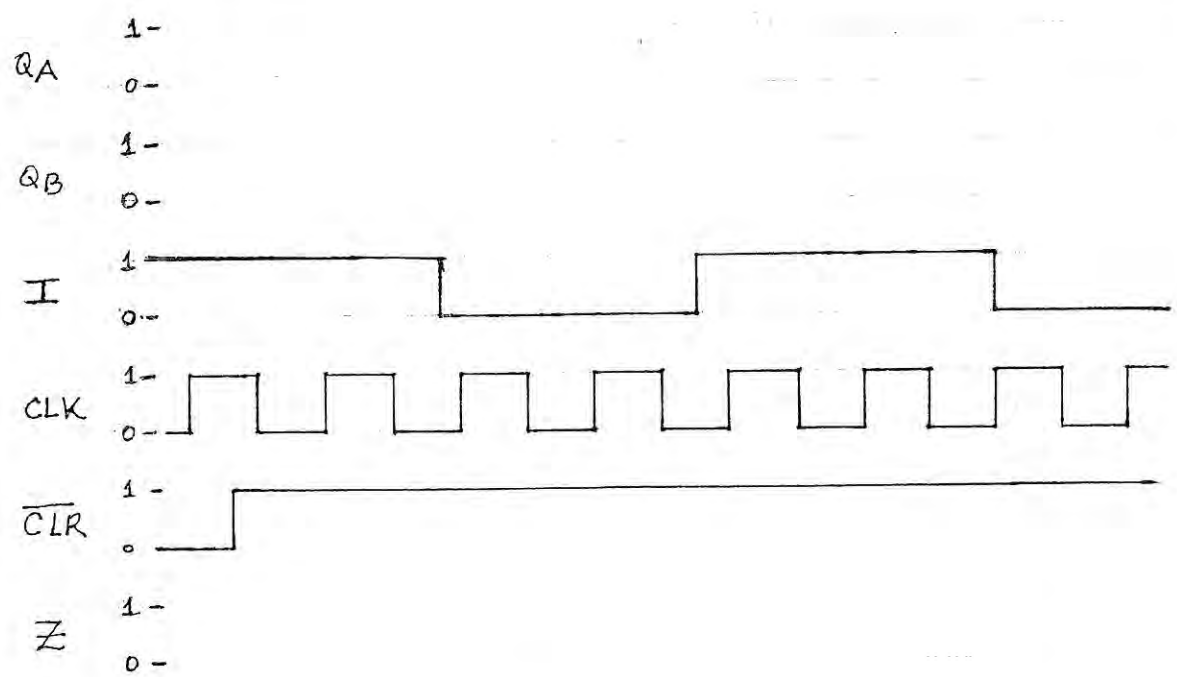
- (a) Design a 3-bit synchronous counter that goes through the sequence 000, 001, 010, 011, 100, 101, 110, 111 and then repeats. Use positive-edge-triggered JK flip-flops. Label the bits  $Q_C$ ,  $Q_B$  &  $Q_A$  where  $Q_C$  is the most significant bit. Draw the circuit implementing the counter. [9 pts]
- (b) Modify the circuit so that it counts whenever an additional COUNT ENABLE (CTE) input is HIGH, stops counting when CTE goes LOW and resumes counting from where it stopped when CTE goes HIGH again. [3 pts]

3.- The finite state machine (FSM) shown in the figure below is implemented with one toggle (T) flip-flop and one D flip-flop. It has a single input I and a single output Z. The combinational logic required is implemented by an 8:1 MUX, 1 NAND and 1 AND gates.

- (a) Is this a Moore or a Mealy FSM? Justify. [2 pts]
- (b) Write the logic expressions for  $T_A$ ,  $D_B$  and Z. [3 pts]
- (c) Obtain the state transition table including  $T_A$ ,  $D_B$ ,  $Q_A^+$ ,  $Q_B^+$  and the output Z. [5 pts]
- (d) Draw the state transition diagram of the FSM including input I and output Z values. [3 pts]



(e) Assuming that the preset input  $\overline{PR}$  is not asserted fill the timing diagram below for  $Q_A$ ,  $Q_B$  and Z. [3 pts]



4.- The diagram below shows the use a D flip-flop governing two digital switches in order to route line PD<sub>0</sub> of the HC11 microcontroller unit (MCU) to one of two connectors: the HOST computer I/O port or the MCU I/O port connector.

Digital switches close when control input C is at a logic '1' and remain open when C is '0'.

HC11 address lines A<sub>15</sub> - A<sub>13</sub> are connected to the 3 address inputs of a 3:8 decoder as shown in the figure, the most significant address input of the decoder is A<sub>2</sub> and the least significant is A<sub>0</sub>. Assume the decoder is enabled and towards the end of the execution of each instruction cycle all its active-low outputs  $\bar{Y}_0 - \bar{Y}_7$  go back to their inactive logic '1' state.

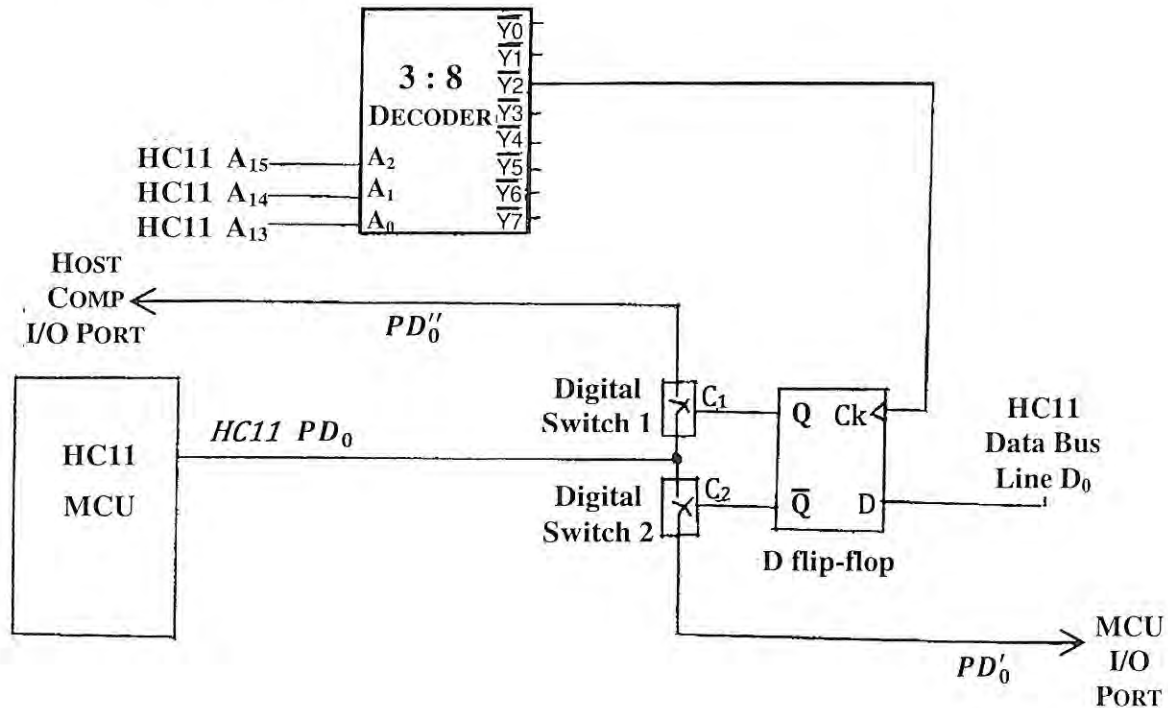
The least significant data bus line of the HC11 (D<sub>0</sub>) is connected to the flip-flop D input.

Knowing that instruction


**ldaa #\$xx** means load HC11 CPU register accumulator A with hexadecimal value **xx**, and **staa \$zzzz** means store the value in accumulator A to address **\$zzzz**,

which of the following set of instructions will direct HC11 line PD<sub>0</sub> to the HOST computer I/O port, which to the MCU I/O port connector and which will not affect the current routing. Mark your choice with an **X** and justify your selection in each case.

- (a) ldaa #\$10, staa \$8000     HOST Comp I/O port,     MCU I/O port,     No Action
- (b) ldaa #\$29, staa \$4000     HOST Comp I/O port,     MCU I/O port,     No Action
- (c) ldaa #\$B4, staa \$5000     HOST Comp I/O port,     MCU I/O port,     No Action
- (d) ldaa #\$05, staa \$2500     HOST Comp I/O port,     MCU I/O port,     No Action



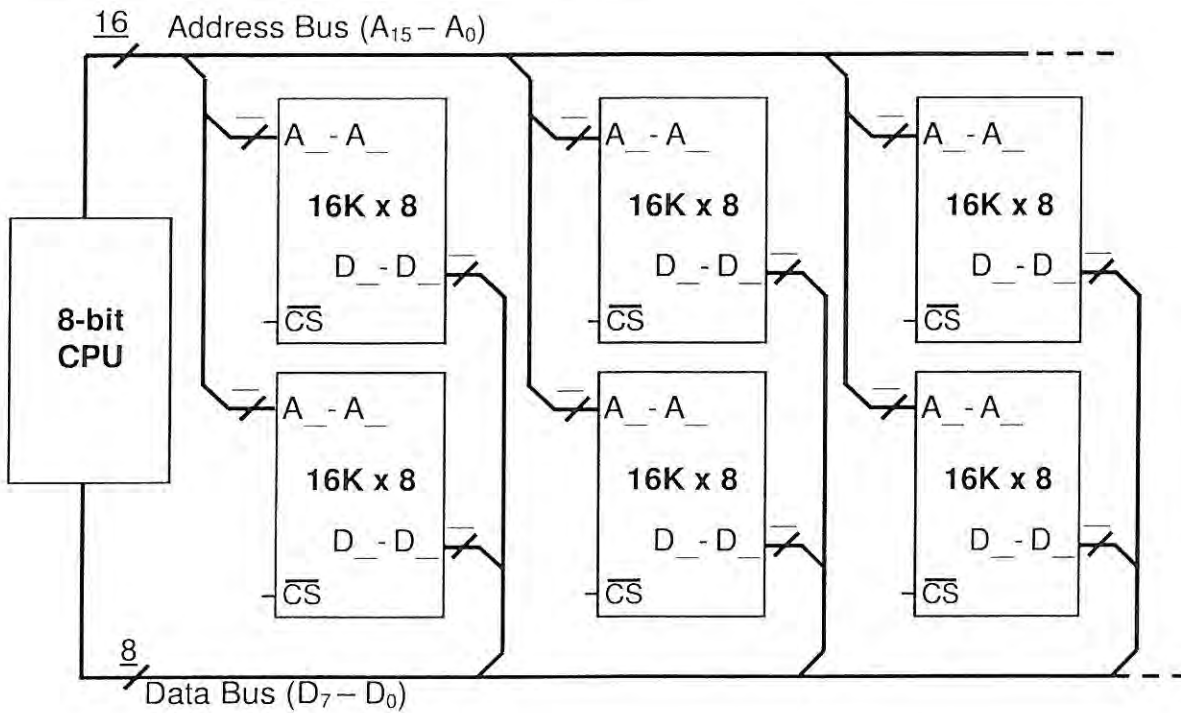
5.- Provide this 8-bit CPU with a 64Kbyte memory space by making use of 16K x 4 memory chips like the ones provided in the figure below.

(a) Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers. The number on top of this symbol  represents the number of lines on that bus. The spaces besides the A's and the D's are to indicate which lines of the address and data busses are connected to each chip, respectively. [6 pts]

(b) Complete the connections in the figure below adding logic gates where needed to produce the chip select ( $\overline{CS}$ ) signals needed in the decoding logic. Explain the reasons for the connections made, include expressions for the Boolean logic used. [6 pts]

(c) Provide the address range allocated to each of the chips used. [4 pts]

Note:  $R/\overline{W}$  & clock signals are omitted for simplicity.



- 6.- (a) Identify the three basic logic gates.  
Is it possible to realize any combinational logic function using just one type of gate?  
Explain. [3 pts]
- (b) What is the main difference between combinational and sequential circuits? [3 pts]
- (c) What is a finite state machine (FSM)?  
Is a counter a special case of FSM? Explain. [3 pts]
- (d) Identify the difference between synchronous and asynchronous counters.  
How would you identify one type or the other? [3 pts]

Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	<u>Identity</u>	<u>Comments</u>
1.	$A + 0 = A$	Operations with 0 and 1
2.	$A + 1 = 1$	Operations with 0 and 1
3.	$A + A = A$	Idempotent
4.	$A + \bar{A} = 1$	Complementarity
5.	$A \cdot 0 = 0$	Operations with 0 and 1
6.	$A \cdot 1 = A$	Operations with 0 and 1
7.	$A \cdot A = A$	Idempotent
8.	$A \cdot \bar{A} = 0$	Complementarity
9.	$\bar{\bar{A}} = A$	Involution
10.	$A + B = B + A$	Commutative
11.	$A \cdot B = B \cdot A$	Commutative
12.	$A + (B + C) = (A + B) + C = A + B + C$	Associative
13.	$A \cdot (B \cdot C) = (A \cdot B) \cdot C = A \cdot B \cdot C$	Associative
14.	$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$	Distributive
15.	$A + (B \cdot C) = (A + B) \cdot (A + C)$	Distributive
16.	$A + (A \cdot B) = A$	Absorption
17.	$A \cdot (A + B) = A$	Absorption
18.	$(A \cdot B) + (\bar{A} \cdot C) + (B \cdot C) = (A \cdot B) + (\bar{A} \cdot C)$	Consensus
19.	$\overline{A + B + C + \dots} = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \dots$	De Morgan
20.	$\overline{A \cdot B \cdot C \cdot \dots} = \bar{A} + \bar{B} + \bar{C} + \dots$	De Morgan
21.	$(A + \bar{B}) \cdot B = A \cdot B$	Simplification
22.	$(A \cdot \bar{B}) + B = A + B$	Simplification