National Exams May 2015

98-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is a OPEN BOOK exam.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Question 1 (20 marks)

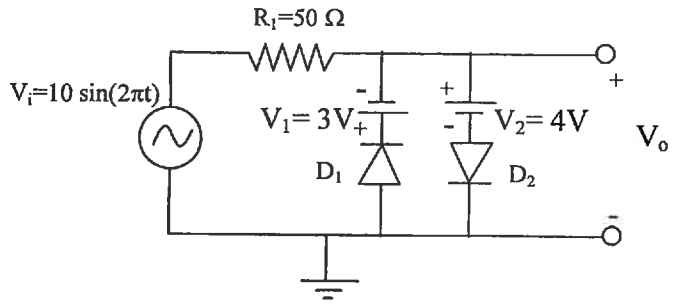

Figure 1. The diodes have a voltage drop V_D=0.7V in forward bias.

For the circuit shown in Figure 1:

a) Sketch V_i and V_o as a function of time, indicating peak voltages.

b) How should D_1 be rated for power consumption?

c) What is the peak current in R_1?

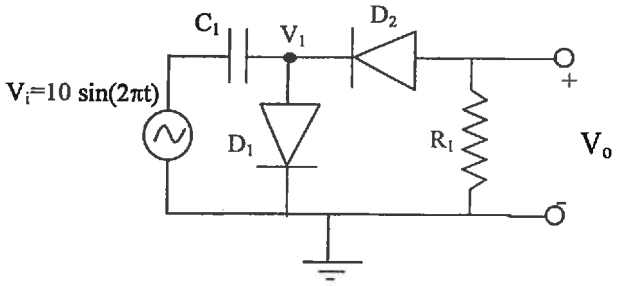

Figure 2. The diodes have a voltage drop V_D=0.7V in forward bias.

For the circuit shown in Figure 2:

d)) Sketch the output waveform $V_o(t)$ in steady state. Label key voltages and times, and indicate changes in operating region for the diodes.

Question 2 (20 marks)

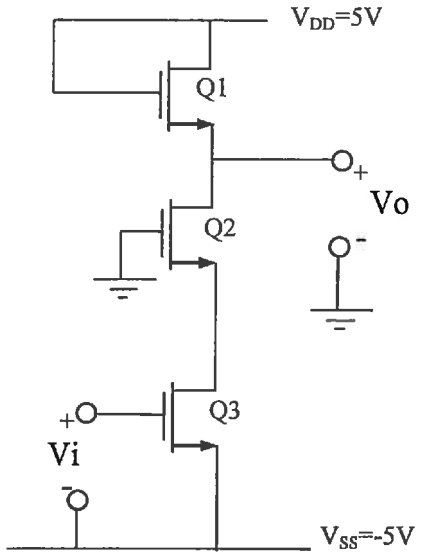

Figure 3. $k_n' = \mu_n C_{ox}$=1 mA/V^2, W/L=10, V_{tn}=1V, $|V_A|$=100V

For the circuit shown in Figure 3:

a) For Vi=2V what is the current through Q3?

b) What is V_{DS} for Q1?

c) Draw a small signal equivalent model for the circuit.

d) What is the small signal AC gain of the circuit?

Question 3 (20 marks)

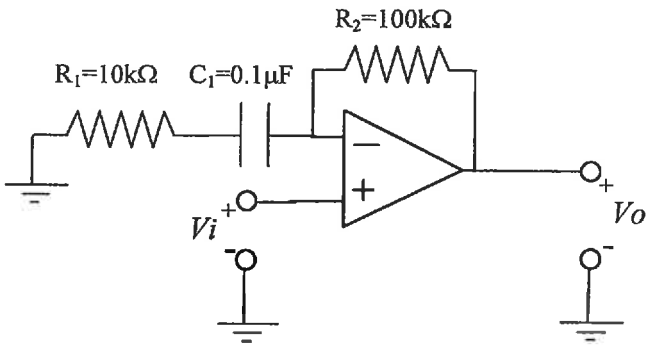

Figure 4.

For the circuit shown in Figure 4:

a) Derive the transfer function $\frac{Vo(j\omega)}{Vi(j\omega)}$ for the circuit shown in Figure 4, assuming the op-amp is ideal.

b) Sketch the frequency response, indicating the 3dB frequency for this circuit.

c) If $V_i(t)$=10sin(120πt) V, find $V_o(j\omega)$.

d) If $V_i(t)$=10sin(120πt) V, find $V_o(t)$.

Question 4(20 marks)

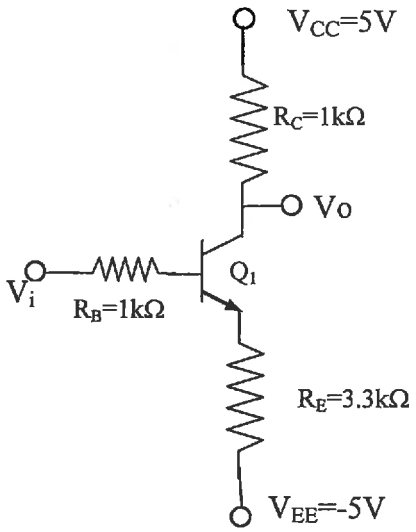

Figure 5. V_{be}=0.7V (active), V_{ce}=0.2V (saturation), β=100.

For the circuit shown in Figure 5:

a) If V_i=0V DC, find the DC bias point for Q1?

b) Draw the small signal equivalent circuit and evaluate the small signal AC voltage gain.

c) Sketch I_c vs V_{ce} and show the operating point for the transistor.

d) How would you change the bias to obtain maximum signal swing?

Question 5 (20 marks)

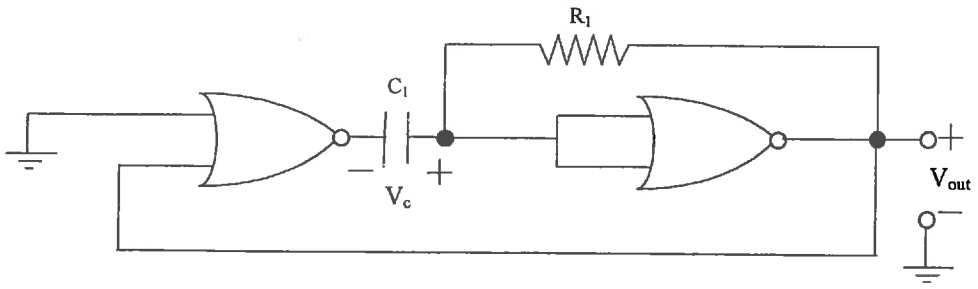

Figure 6. Assume the gates are ideal and switch at $V_{DD}/2$.

For the circuit shown in Figure 6:

a) Explain the operation of this circuit.

b) Sketch the waveforms $V_c(t)$ and $V_{out}(t)$.

c) Find an expression for $V_c(t)$.

d) Find the period of the waveform if R_1=10 kΩ and C_1=10 nF.

Question 6 (20 marks)

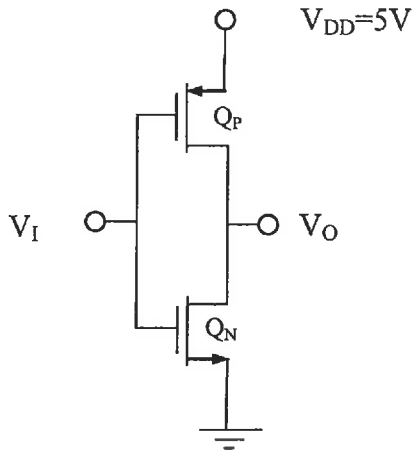

Figure 7. k_n'=50 μA/V^2, k_p'=20 μA/V^2, V_{tn}=-V_{tp}=1V, C_{ox}=1fF/μm^2, V_{DD}=5V.

a) If the minimum gate length for this technology is 1 μm, size Q_N and Q_P to obtain a symmetric transfer characteristic.

b) Estimate the maximum capacitance this circuit can drive with a propagation delay of less than 200 ps.

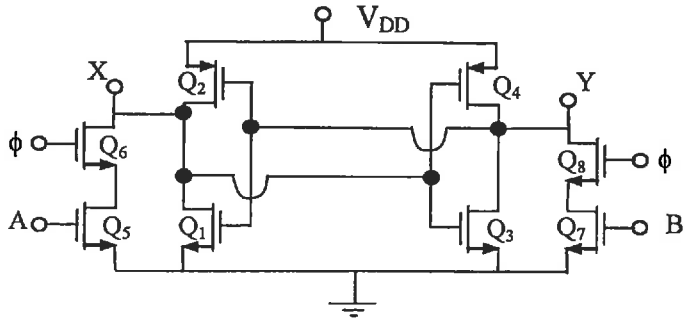

Figure 8.

For the circuit shown in Figure 8:

c) Determine outputs X and Y for all possible inputs A and B. ϕ is a clock signal.

d) If Q_1 and Q_2 are sized as in part a), find a minimum size for Q_5 and Q_6 that will ensure X can be pulled down to V_{DD}/2 or lower.

Question 7 (20 marks)

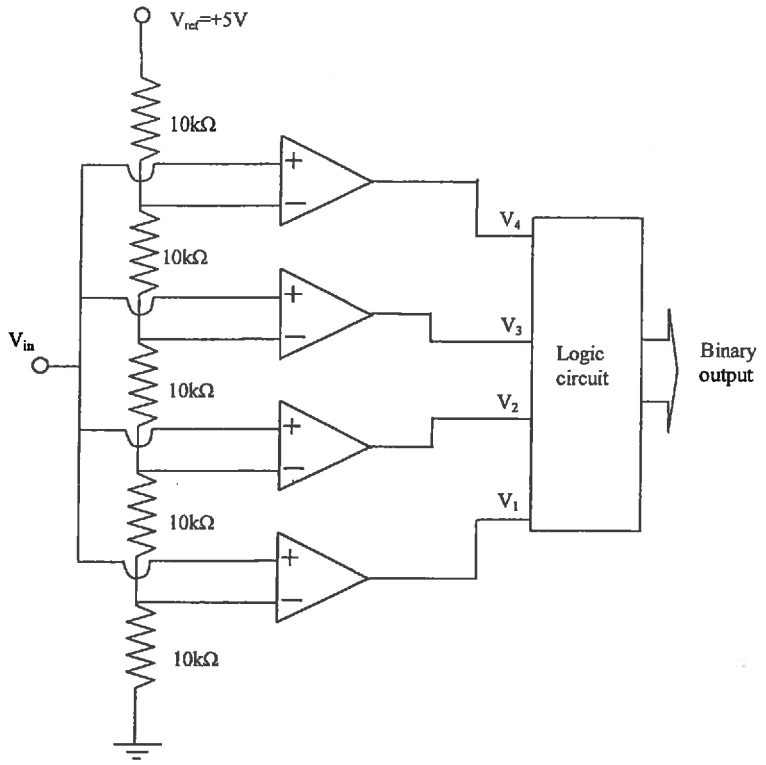

Figure 9.

a) What is a common name for the ADC circuit shown in Figure 9? What is a principal advantage of this circuit over other ADC implementations?

b) What are the analog voltages at each of the comparator negative inputs? If V_{in}=3V what are the logic values for V_1 through V_4?

c) List all possible combinations of V_1-V_4 and the corresponding binary output.

d) In an integrated circuit, how could V_{ref} be generated?

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (4 parts, 5 marks each)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (4 parts, 5 marks each)
5. 20 marks total (4 parts, 5 marks each)
6. 20 marks total (4 parts, 5 marks each)
7. 20 marks total (4 parts, 5 marks each)